6+3 channels PMIC

Features

- **3.0V ~ 5.5V Input Voltage Operation.**
- **95% Efficient DC/DC Converter**
- **Built-in 6-ch synchronous buck converter, 3-ch LDOs**
- **Bucks and LDOs can be set to lower Iq at low load.**
- **Buck2, Buck3, Buck5 and Buck6 Supports DVS Function, 12.5mV/step.**
- **Built-In Power ON/OFF Sequence for PMU.**
- **Built-In Short Circuit Protection (SCP), Under Voltage Protection (UVP), and cycle-by cycle current limit for DC/DC Converters.**
- **LDOs are Programmable to Voltage Options by I^2C.**
- **Built-In Thermal Shutdown Function.**
- **Built-In VCC OVP Function.**
- **TQFN5X5-32 Package**

General Description

The G2227 provide a complete power supply solution for handsets or data card. It contains 6 dc/dc converters and 3 LDOs to power each critical blocks of mobile phone, and is optimized for maximum battery life, featuring a low ground current when in standby mode operation. All channels DC/DC converters operate at one fixed frequency of 3.0MHz to optimize size, cost, and efficiency. All Synchronous converters operate at pulse skipping mode at light load. The G2227 features a I^2C compatible interface.

The G2227 is available in TQFN5X5-32 package.

Applications

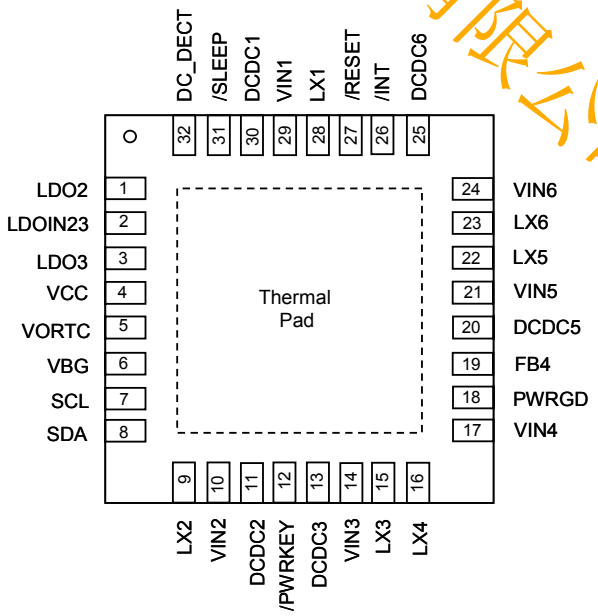
- **Mobile Handsets**
- **TV Dongle**
- **Smart Phone**
- **Set Top Box**

Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
G2227RA1U	2227	-40°C~+85°C	TQFN5X5-32

Note: RA:TQFN5X5-32
1: Bonding code
U: Tape & Reel
Green : Lead Free / Halogen Free

Pin Configuration



G2227 TQFN5X5-32

Note: Recommend connecting the Thermal Pad to the Ground for excellent power dissipation.

Absolute Maximum Ratings

VCC, VIN1, VIN2, VIN3, VIN4, VIN5, VIN6, LDOIN23 . . . . . -0.3V to +6.3V
DCDC1, DCDC2, DCDC3, FB4, DCDC5, DCDC6, VORTC, LDO2, LDO3 . . . . . -0.3V to +6.3V
LX1, LX2, LX3, LX4, LX5, LX6 . . . . . -0.3V to +6.3V
Other Pins . . . . . -0.3V to +6.3V
Thermal Resistance Junction to Ambient, (θ_{JA})
TQFN5X5-32 . . . . . 23°C/W
Continuous Power Dissipation (T_A=25°C)
TQFN5X5-32. . . . . 6.5W
Thermal Resistance Junction to Case, (θ_{JC})
TQFN5X5-32 . . . . . 7°C/W
Operating Ambient Temperature .-35°C to 85°C
Storage Temperature Range. . . . . -55°C to +150°C
Reflow Temperature (soldering, 10 sec) . . . . . 260°C
EDS Susceptibility (Human Body Mode) 2kV
EDS Susceptibility (Machine Mode) 200V

1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Device are ESD sensitive. Handling precaution recommended. The Human Body model is a 100pF capacitor discharged through a 1.5KΩ resistor into each pin.

Electrical characteristics

(VCC=VINx=3.7V, LDOINx=3.7V, T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL						
VCC Operating Voltage for PMU	V_{VCC_PMU}		3.0	---	5.5	V
VCC Over Voltage threshold	V_{VCC_OVLO}	VCC rising	5.8	6.0	---	V
VCC Under Voltage threshold	V_{VCC_UVLO}	VCC falling	---	3.0	---	V
VCC Under Voltage Hysteresis	$V_{VCC\_UVLOHYS}$			500		mV
PMU Stand-by Supply Current	I_{VCC}	ALL converters enter ECO mode, and without loading current.	---	---	200	uA
OSCILLATOR						
Frequency	F_{OSC}	DCDC1~DCDC6	2.6	3.0	3.4	MHz
DCDC1 Buck Converter						
Soft-Start Internal	SS_CH1		---	2	---	mS
VO1 regulation voltage accuracy	%VO1		-1.5	---	1.5	%
Maximum Duty Cycle	D_{max1}		---	100	---	%
VIN1 Leakage Current	I_{VIN1_LK}	V_{LX1}=0V, VIN1=5.0V	---	1	5	μA
LX1 Leakage Current	I_{LX1_LK}	V_{LX1}=5.0V	---	1	5	μA
Switch ON Resistance	Ron1-N		---	120	---	mΩ
	Ron1-P		---	150	---	
Peak Current Limit	I_{LIM_CH1}		2.5	2.8	---	A
Under Voltage Protection Threshold	$\%V_{UVP\_CH3}$	Ratio=V_{UVP}/V_{OUT}	---	75	---	%
DCDC2 Buck Converter						
Soft-Start Internal	SS_CH2		---	2	---	mS
VO2 regulation voltage accuracy	%VO2		-1.5	---	1.5	%
Maximum Duty Cycle	D_{max2}		---	100	---	%
VIN2 Leakage Current	I_{VIN2_LK}	V_{LX2}=0V, VIN2=5.0V	---	1	5	μA
LX2 Leakage Current	I_{LX1_LK}	V_{LX2}=5.0V	---	1	5	μA
Switch ON Resistance	Ron2-N		---	70	---	mΩ
	Ron2-P		---	120	---	
Peak Current Limit	I_{LIM_CH2}		3.5	4.0	---	A
Under Voltage Protection Threshold	ΔV_{UVP_CH2}	$\Delta V_{UVP\_CH2}=VOUT_{SET}-VOUT_{UVP}$	---	100	---	mV

Electrical characteristics (continued)

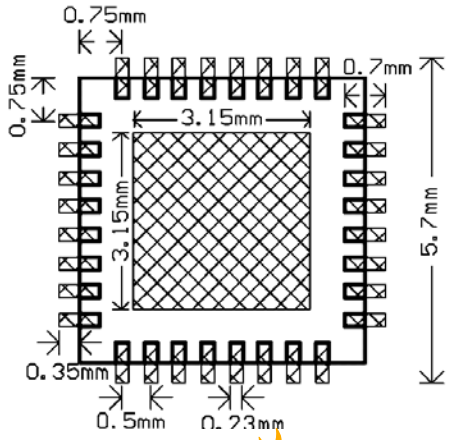
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
DCDC3, DCDC5, DCDC6 Buck Converter						
Soft-Start Internal	SS_CHx		---	2	---	mS
VO regulation voltage accuracy	%VOx		-1.5	---	1.5	%
Maximum Duty Cycle	D_{maxx}		---	100	---	%
VINx Leakage Current	I_{VINx_LK}	V_{LXx}=0V, VINx=5.0V	---	1	5	μA
LXx Leakage Current	I_{LXx_LK}	V_{LXx}=5.0V	---	1	5	μA
Switch ON Resistance	Ronx-N		---	120	---	mΩ
	Ronx-P		---	150	---	
Peak Current Limit	I_{LIM_CHx}		2.5	2.8	---	A
Under Voltage Protection Threshold	ΔV_{UVP_CHx}	ΔV_{UVP_CHx}=$VOUT_{SET}$-$VOUT_{UVP}$	---	100	---	mV
DCDC4 Buck Converter						
Soft-Start Internal	SS_CH4		---	2	---	mS
FB pin regulation voltage	V_{FB}		0.788	0.80	0.812	V
Maximum Duty Cycle	D_{max4}		---	100	---	%
VIN Leakage Current	I_{VIN4_LK}	V_{LX4}=0V, VIN4=5.0V	---	1	5	μA
LX Leakage Current	I_{LX4_LK}	V_{LX4}=5.0V	---	1	5	μA
Switch ON Resistance	Ron4-N		---	120	---	mΩ
	Ron4-P		---	150	---	
Peak Current Limit	I_{LIM_CH4}		2.5	2.8	---	A
Under Voltage Protection Threshold	$\%V_{UVP\_CH4}$	Ratio=V_{UVP}/V_{OUT}	---	90	---	%
RTCLDO						
Input voltage range	V_{VINRTC}	VCC	2.5	---	5.5	V
Standby current	I_{Q1_RTC}	V_{VCC}=3.7v	---	5	8	μA
Output voltage	V_{RTCO}	Io=0.1mA, VORTC=2'b01	3.05	3.1	3.15	V
Dropout Voltage	V_{DO1_RTC}	Io=50mA, VORTC=2'b01	---	---	800	mV
	V_{DO2_RTC}	Io=10mA, VORTC=2'b01	---	---	150	mV
Maximum Output Current		V_{VCC}=4.2V, RTCOUT=95%*V_{SET}	60	---	200	mA
LDO2, LDO3						
Input voltage range	V_{LDOINC}	LDOIN23	2.8	---	5.5	V
Soft-Start Internal	SS_{LDOC}		---	2	---	mS
Output Voltage accuracy	$\%V_{LDOC}$	Io=100mA,	-1.5	---	1.5	%
Continuous output current at ECO mode	I_{OC_ECO}				5	mA
LDO Input Current	I_{LDOINC}	Io=0mA, Normal mode	---	---	32	μA
	I_{LDOINC_ECO}	Io=0mA, ECO mode			8	μA
Dropout Voltage	V_{DOLDOC}	Io=300mA, Normal mode	---	200	400	mV
	$V_{DOLLDOC}$	Io=50mA, Normal mode		35	70	mV
Output current limit	$I_{LIMLDOC}$	LDOIN23>LDOx+1.0V, , Normal mode	550	600	---	mA
LDO Load Regulation	$\%LD_C$	LDOIN23>LDOx+1.0V, Normal mode Io=1mA~200mA	---	---	1	%
Short Circuit Protection threshold	$\%V_{SCPLDOC}$	Ratio=V_{SCP}/V_{OUT}	---	12.5	---	%
Ripple Rejection	$PSRR_C$	f=10Hz~3kHz, Io=100mA, Normal mode	---	65	---	dB
Output Noise Voltage		f=10Hz~100kHz, Normal mode	---	45	---	uVrms
ECO exit time	t_{d_ECO}	Minimum wait time to draw full current after leaving ECO mode	---	---	50	uS

Electrical characteristics (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Protection						
UVP Protection Fault Delay	t_{D_Fault}	DCDC1~DCDC6	128	---	---	mS
Thermal Shutdown Detect	T_{SD}		---	150	---	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		---	20	---	°C
DCIN Detection						
DC_DECT detection Voltage Threshold	V_{DCDET}	DC_DECT rising		1.2		V
DC_DECT detection Voltage Hysteresis	$V_{DCDETHS}$	DC_DECT falling		100		mV
Control Signal						
Logic-Input Threshold (/PWRKEY,/SLEEP,/RESET)	V_{TH}	High threshold	1.4	---	---	V
	V_{TL}	Low threshold	---	---	0.5	V
Pull High Resistance (/PWRKEY,/SLEEP, and /RESET)	R_{PH}		---	100	---	KΩ
Open-Drain Output Low Voltage (PWRGD,/INT,)	V_{ODLOW}	I_{SINK}=5mA, V_{VCC}=3.7V	---	---	100	mV
Open-Drain Output Leakage Current (PWRGD./INT)	I_{LK_OD}	V_{OD}=5V	---	---	1	µA
PWRGD Delay Time	t_{RDLY_PWRGD}			8		mS
Re-start up Delay Time	$t_{DLY\_REBOOST}$			1		Sec
SMBus Interface						
Logic Input High Voltage	V_{IH}	SCL, SDA	1.4	---	---	V
Logic Input Low Voltage	V_{IL}	SCL, SDA	---	---	0.5	V
Logic Input Current		Logic inputs forced to VCC or GND	-2	---	2	µA
SMBus Input Capacitance		SCL, SDA	---	5	---	pF
SMBus Clock Frequency	f_{SCL}	Fast mode	---	---	400	kHz
		High-speed mode, load 400pF max			1.7	MHz
		High-speed mode, load 100pF max			3.4	MHz
SCL Clock Low Time	t_{LOW}	Fast mode	1.3	---	---	µS
SCL Clock High Time	t_{HIGH}	Fast mode	0.6	---	---	µS
SDA Setup Time	$t_{SU:\ DAT}$	Fast mode	100			nS
SDA Hold Time	$t_{HD\ :\ DAT}$	Fast mode	0		0.9	uS
Bus-Free Time from START and STOP	t_{BUF}	Fast mode	1.3	---	---	µS
Hold Time Repeated START Condition	$t_{HD:\ STA}$	Fast mode	0.6	---	---	µS
Setup Time Repeated START Condition	$t_{SU\ :\ STA}$	Fast mode	0.6	---	---	µS
Setup Time for STOP Condition	$t_{SU;STO}$	Fast mode	0.6	---	---	µS
Rise Time of SCL/SDA signals	t_r	10% to 90% points	20	---	300	nS
Fall Time of SCL/SDA signals	t_f	90% to 10% points	20	---	300	nS

Minimum Footprint PCB Layout Section

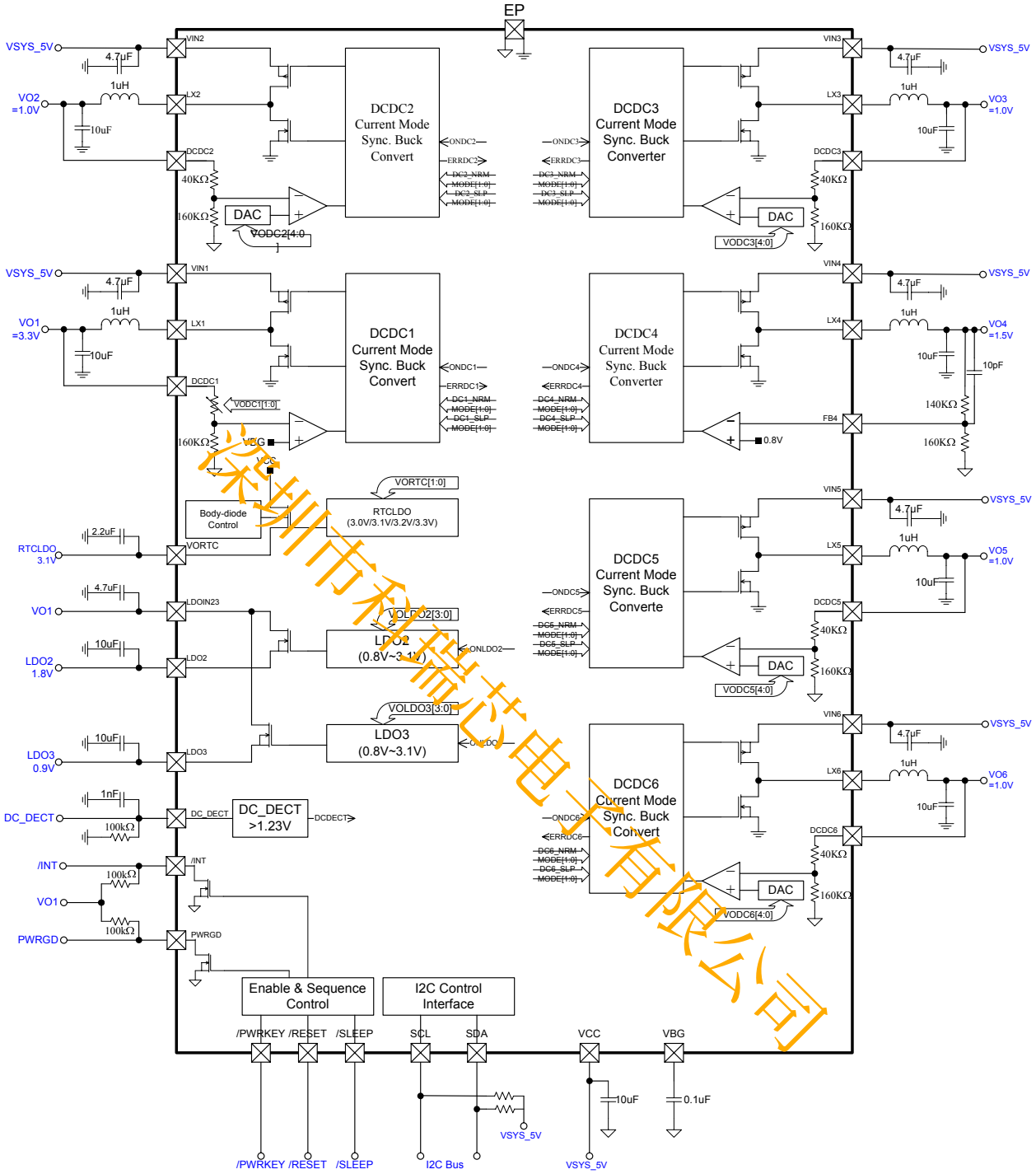
TQFN5X5-32



Pin Description

Pin No	Pin Name	Function
1	LDO2	LDO Output of LDO2.
2	LDOIN23	Power Input of LDO2 and LDO3.
3	LDO3	LDO Output of LDO3.
4	VCC	IC Power Supply Input pin. Bypass with a 10uF or greater ceramic capacitor.
5	VORTC	LDO Output of RTC LDO. Bypass this pin to ground with a 2.2uF ceramic capacitor.
6	VBG	1.23v Reference Voltage Output. Bypass this pin to ground with a 0.47uF ceramic capacitor.
7	SCL	Clock Input PIN of I^2C interface.
8	SDA	Data Input PIN of I^2C interface.
9	LX2	Inductor switch node of DCDC2 Buck Converter.
10	VIN2	Power Input of DCDC2 Buck Converter.
11	DCDC2	Sensing Input of DCDC2 Buck Converter's output voltage.
12	/PWRKEY	Power on/off key. Internal pull high to VCC.
13	DCDC3	Sensing Input of DCDC3 Buck Converter's output voltage.
14	VIN3	Power Input of DCDC3 Buck Converter.
15	LX3	Inductor switch node of DCDC3 Buck Converter.
16	LX4	Inductor switch node of DCDC4 Buck Converter.
17	VIN4	Power Input of DCDC4 Buck Converter.
18	PWRGD	Indicator of PMU power on/off with open drain output.
19	FB4	Feedback Input of DCDC4 Buck Converter.
20	DCDC5	Sensing Input of DCDC5 Buck Converter's output voltage.
21	VIN5	Power Input of DCDC5 Buck Converter.
22	LX5	Inductor switch node of DCDC5 Buck Converter.
23	LX6	Inductor switch node of DCDC6 Buck Converter.
24	VIN6	Power Input of DCDC6 Buck Converter.
25	DCDC6	Sensing Input of DCDC6 Buck Converter's output voltage.
26	/INT	Interrupt Indicator with open drain output.
27	/RESET	RESET PIN of G2227. Internal pull high to VCC.
28	LX1	Inductor switch node of DCDC1 Buck Converter.
29	VIN1	Power Input of DCDC1 Buck Converter.
30	DCDC1	Sensing Input of DCDC1 Buck Converter's output voltage.
31	/SLEEP	SLEEP mode control pin. Internal pull high to VCC.
32	DC_DECT	DCIN Input PIN, must not be left open.
EP	AGND, PGNDX	All converters' power ground and chip analog ground. For good thermal dissipation, connect EP to the power and analog ground plane.

Block Diagram & Application Circuit



I2C Interface

G2227 I2C slave address=7'b0010010. The write or read bit stream (N≥1) is shown below:

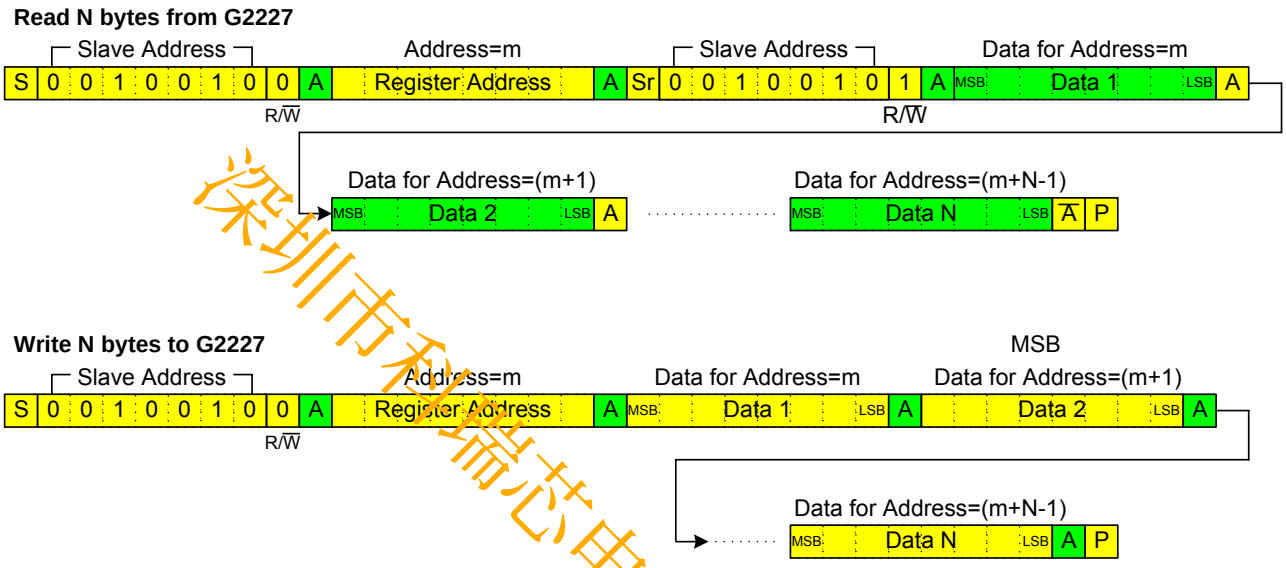
Driven by Master

Driven by G2227

S Start

P Stop

Sr Repeat Start



I2C Register Map

ADDR	Byte Name		Data							
			b7	b6	b5	b4	b3	b2	b1	b0
0x00	INTR	Meaning	INT		PWRKEY	PWRKEY_LP	PWRKEY_IT			DCDECT
		Default	0		0	0	0			0
		Read/Write	R/W		R	R	R			R
0x01	INTR _MASK	Meaning			MASK _PWRKEY	MASK_LP	MASK_IT			MASK_ DCDECT
		Default			0	0	0			0
		Read/Write			R/W	R/W	R/W			R/W
0x02	PWRKEY Control	Meaning	LPOFF_TO_ DO	ENLPOFF	TIME_IT[1:0]		TIME_LP[1:0]		TIME_LPOFF[1:0]	
		Default	1	1	0	0	0	1	1	1
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0x03	DCDC Fault Status	Meaning	ERRDC1	ERRDC2	ERRDC3	ERRDC4	ERRDC5	ERRDC6	ERRLDO2	ERRLDO3
		Default	0	0	0	0	0	0	0	0
		Read/Write	R	R	R	R	R	R	R	R
0x04	SYS _Control	Meaning	SOFTOFF				RST_ERR		VORTC[1:0]	
		Default	0				0		0	1
		Read/Write	R/W				R/W		R/W	R/W
0x05	DCDC&LDO _ONOFF CONTROL	Meaning	ONDC1	ONDC2	ONDC3	ONDC4	ONDC5	ONDC6	ONLDO2	ONLDO3
		Default	1	1	1	1	1	1	1	1
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0x06	DCDC&LDO _DISCHG CONTROL	Meaning	ENDIS_DC1	ENDIS_DC2	ENDIS_DC3	ENDIS_DC4	ENDIS_DC5	ENDIS_DC6	ENDIS_L2	ENDIS_L3
		Default	1	1	1	1	1	1	1	1
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0x07	DC1DC2 _MODE CONTROL	Meaning	DC1_NRMMODE[1:0]		DC1_SLPMODE[1:0]		DC2_NRMMODE[1:0]		DC2_SLPMODE[1:0]	
		Default	0	0	1	0	0	0	1	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0x08	DC3DC4 _MODE CONTROL	Meaning	DC3_NRMMODE[1:0]		DC3_SLPMODE[1:0]		DC4_NRMMODE[1:0]		DC4_SLPMODE[1:0]	
		Default	0	0	1	0	0	0	1	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0x09	DC5DC6 _MODE CONTROL	Meaning	DC5_NRMMODE[1:0]		DC5_SLPMODE[1:0]		DC6_NRMMODE[1:0]		DC6_SLPMODE[1:0]	
		Default	0	0	1	0	0	0	1	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0x0A	LDO2LDO3 _MODE CONTROL	Meaning	LDO2_NRMMODE[1:0]		LDO2_SLPMODE[1:0]		LDO3_NRMMODE[1:0]		LDO3_SLPMODE[1:0]	
		Default	0	0	1	0	0	0	1	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0x10	DCDC2 _NRMVOLT	Meaning				VODC2_NRM[4:0]				
		Default				1	0	0	0	0
		Read/Write				R/W	R/W	R/W	R/W	R/W
0x11	DCDC3 _NRMVOLT	Meaning				VODC3_NRM[4:0]				
		Default				1	0	0	0	0
		Read/Write				R/W	R/W	R/W	R/W	R/W
0x12	DCDC5 _NRMVOLT	Meaning				VODC5_NRM[4:0]				
		Default				1	0	0	0	0
		Read/Write				R/W	R/W	R/W	R/W	R/W
0x13	DCDC1&6 _NRMVOLT	Meaning	VODC1_NRM[1:0]				VODC6_NRM[4:0]			
		Default	1	1		1	0	0	0	0
		Read/Write	R/W	R/W		R/W	R/W	R/W	R/W	R/W
0x14	LDO _NRMVOLT	Meaning	VOLDO2_NRM[3:0]				VOLDO3_NRM[3:0]			
		Default	1	0	1	0	0	0	1	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0x15	DCDC2 _SLPVOLT	Meaning				VODC2_SLP[4:0]				
		Default				1	0	0	0	0
		Read/Write				R/W	R/W	R/W	R/W	R/W
0x16	DCDC3 _SLPVOLT	Meaning				VODC3_SLP[4:0]				
		Default				1	0	0	0	0
		Read/Write				R/W	R/W	R/W	R/W	R/W
0x17	DCDC5 _SLPVOLT	Meaning				VODC5_SLP[4:0]				
		Default				1	0	0	0	0
		Read/Write				R/W	R/W	R/W	R/W	R/W
0x18	DCDC1&6 _SLPVOLT	Meaning	VODC1_SLP[1:0]				VODC6_SLP[4:0]			
		Default	1	1		1	0	0	0	0
		Read/Write	R/W	R/W		R/W	R/W	R/W	R/W	R/W
0x19	LDO _SLPVOLT	Meaning	VOLDO2_SLP[3:0]				VOLDO3_SLP[3:0]			
		Default	1	0	1	0	0	0	1	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0x20	VERSION	Meaning	CHIP_ID[4:0]					VERSION[2:0]		
		Default	1	1	0	1	1	0	0	0
		Read/Write	R	R	R	R	R	R	R	R
0xF1	GMT Testing	Meaning					TM[5:1]			
		Default				0	0	0	0	0
		Read/Write				R/W	R/W	R/W	R/W	R/W

I2C Register Reset Conditions

ADDR.	Register Function	Rest Condition
0x00	Interrupt Registers	VCC<1.3V, or the power-off reset pulse. Also reset by reading them
0x02	Power-key IT/LP/LPOFF Registers	VCC<1.3V, or the power-on leading pulse
0x03,0x04[3]	DCDC&LDO Fault Status	VCC<1.3V or 0x04[3] is written to 1
0x04[7]	SOFTOFF	VCC<1.3V, or the power-on leading pulse
0x06	DCDC and LDO enable discharge Registers	VCC<1.3V, or the power-on leading pulse
Other Registers		VCC<1.3V, or the power-off reset pulse.

I2C Register Function Table

Interrupt and Status

ADDR	Data Bit	Data Name	Function Description
0x00	b7	INT	INT is used to control the output status of /INT pin. When interrupt events happen, /INT pin goes low and this bit is set to 1'b1. After Micro-processor write the bit to be 1'b0, /INT pin goes to high-Z state. INT: 0 = Hi-Z; 1 = Low
0x00	b5	PWRKEY	PWRKEY is used to record the /PWRKEY pin status has changed since last read.
0x00	b4	PWRKEY_LP	PWRKEY_LP is used to record the /PWRKEY long press status. /PWRKEY_LP is reset to 0 when this byte is read each time .This bit is also reset to 0 at each /PWRKEY falling edge or VCC plug-in/out. PWRKEY_LP: 0 = NO; 1 = YES ($T>T_{dPWRKEYLP}$)
0x00	b3	PWRKEY_IT	PWRKEY_IT is used to record the /PWRKEY falling status. /PWRKEY_IT is reset to 0 when this byte is read each time. This bit is reset to 0 at each /PWRKEY falling edge or VCC plug-in/out. PWRKEY_IT: 0 = NO; 1 = YES ($T>T_{dbPWRKEYF}$)
0x00	b0	DCDECT	DCDECT is used to record the DC_DECT pin status. DCDECT is reset to 0 when this byte is read each time. This bit is reset to 0 at VCC plug-in/out. DCDECT: 0 = NO; 1 = YES (V(DC_DECT)>1.23V)
0x01	b5	MASK _PWRKEY	By writing 1'b1 to MASK_PWRKEY to disable asserting /INT low when the event of /PWRKEY is toggled low occurs.
0x01	b4	MASK_LP	By writing 1'b1 to MASK_LP to disable asserting /INT low when the event of /PWRKEY is toggled low with duration longer than TdPWRKEYLP occurs.
0x01	b3	MASK_IT	By writing 1'b1 to MASK_IT to disable asserting /INT low when the event of /PWRKEY is toggled low duration longer than TdPWRKEYLP occurs.
0x01	B0	MASK _DCDECT	By writing 1'b1 to MASK_DCDET to disable asserting /INT low when the event of DC_DECT occurs.

Software PMIC ON/OFF Control

ADDR	Data Bit	Data Name	Function Description
0x04	b7	SOFTOFF	Write 1 to SOFTOFF to perform power-off sequence when PMIC is in operation mode.

Mode Control of DCDC1~DCDC6

<table>
<tr><th>ADDR</th><th>Data Bit</th><th>Data Name</th><th>Function Description</th></tr>
<tr><td>0x07
0x08
0x09</td><td>b7,b6
b3,b2</td><td>DCx
_NRMMODE
[1:0]</td><td>Setting the operating mode of DCDC1, DCDC2, DCDC3, DCDC4, DCDC5 and DCDC6 when /SLEEP pin is toggled high. Default=2'b00
<table>
<tr><td>DCx_NRMMODE[1:0]</td><td>DCDCx Operating Mode</td></tr>
<tr><td>00</td><td rowspan="2">Auto PWM/PSM with ECO</td></tr>
<tr><td>01</td></tr>
<tr><td>10</td><td>Force PWM</td></tr>
<tr><td>11</td><td>Auto PWM/PSM w/o ECO</td></tr>
</table></td></tr>
<tr><td>0x07
0x08
0x09</td><td>b5,b4
b1,b0</td><td>DC1,DC2,DC3
DC5,DC6
_SLPMODE
[1:0]</td><td>Setting the DCDC1, DCDC2, DCDC3, DCDC5, and DCDC6s' operating mode, and output voltage configuration when /SLEEP pin is toggled low. Default=2'b10
<table>
<tr><td>DCx_SLPMODE[1:0]</td><td>DCDCx Operating Mode</td><td>Output Voltage Configured by</td></tr>
<tr><td>00</td><td>Auto PWM/PSM w/o ECO</td><td>VODCx_NRM[3:0]</td></tr>
<tr><td>01</td><td rowspan="2">Auto PWM/PSM with ECO</td><td>VODCx_NRM[3:0]</td></tr>
<tr><td>10</td><td>VODCx_SLP[3:0]</td></tr>
<tr><td>11</td><td>shutdown</td><td>X</td></tr>
</table></td></tr>
<tr><td>0x08</td><td>b1,b0</td><td>DC4
_SLPMODE
[1:0]</td><td>Setting the operating mode of DCDC4 when /SLEEP pin is toggled low. Default=2'b10
<table>
<tr><td>DC4_SLPMODE[1:0]</td><td>DCDC4 Operating Mode</td></tr>
<tr><td>00</td><td>Auto PWM/PSM w/o ECO</td></tr>
<tr><td>01</td><td rowspan="2">Auto PWM/PSM with ECO</td></tr>
<tr><td>10</td></tr>
<tr><td>11</td><td>shutdown</td></tr>
</table></td></tr>
</table>

Mode Control of LDO2,LDO3

<table>
<tr><th>ADDR</th><th>Data Bit</th><th>Data Name</th><th>Function Description</th></tr>
<tr><td>0x0A</td><td>b7,b6
b3,b2</td><td>LDOx
_NRMMODE
[1:0]</td><td>Setting the LDOs' operating mode and output voltage when /SLEEP pin is toggled high. Default=2'b00
<table>
<tr><td>LDOx_NRMMODE[1:0]</td><td>MODE</td><td>Output Voltage</td></tr>
<tr><td>00</td><td rowspan="2">Normal</td><td rowspan="2">VOLDOx_NRM [3:0]</td></tr>
<tr><td>01</td></tr>
<tr><td>10</td><td>ECO</td><td>VOLDOx_NRM[3:0]</td></tr>
<tr><td>11</td><td>Normal</td><td>VOLDOx_NRM [3:0]</td></tr>
</table></td></tr>
<tr><td>0x0A</td><td>b5,b4
b1,b0</td><td>LDOx
_SLPMODE
[1:0]</td><td>Setting the LDOs' operating mode and output voltage when pin SLEEP is toggled low, Default=2'b10
<table>
<tr><td>LDOx_SLPMODE[1:0]</td><td>MODE</td><td>Output Voltage</td></tr>
<tr><td>00</td><td>Normal</td><td>VOLDOx_NRM [3:0]</td></tr>
<tr><td>01</td><td>Normal</td><td>VOLDOx_SLP [3:0]</td></tr>
<tr><td>10</td><td>ECO</td><td>VOLDOx_SLP[3:0]</td></tr>
<tr><td>11</td><td>Shutdown</td><td>X</td></tr>
</table></td></tr>
</table>

Voltage Control of RTCLDO

<table>
<tr><th>ADDR</th><th>Data Bit</th><th>Data Name</th><th>Function Description</th></tr>
<tr><td>0x04</td><td>b1,b0</td><td>VORTC[1:0]</td><td>Setting the output voltage of RTCLDO, Default=2'b01
<table>
<tr><td>VORTC[1:0]</td><td>VORTC</td></tr>
<tr><td>11</td><td>3.3V</td></tr>
<tr><td>10</td><td>3.2V</td></tr>
<tr><td>01</td><td>3.1V</td></tr>
<tr><td>00</td><td>3.0V</td></tr>
</table></td></tr>
</table>

Voltage Control of DCDC1~DCDC6

ADDR	Data Bit	Data Name	Function Description
0x13 0x18	b7,b6	VODC1 _NRM[1:0] /VODC1 _SLP[1:0]	Setting the output voltage of DCDC1 in Normal/Sleep mode, Default=2'b11 VODC1_[1:0] / VO1 ***11*** / ***3.3V*** 10 / 3.2V 01 / 3.1V 00 / 3.0V
0x10 0x11 0x12 0x13 0x15 0x16 0x17 0x18	b4~b0	VODCx _NRM[3:0] /VODCx _SLP[3:0]	Setting the feedback reference voltage of DCDC2, DCDC3, DCDC5, and DCDC6 in Normal/Sleep mode. VOx=VFBx/0.8, Default=5'b10000 VFBx=0.64V + 10mV x Value, VO2=0.8V + 12.5mV x Value, where Value is 5-bit binary code

FBDC2[4:0]	VFB2	VO2	FBDC2[4:0]	VFB2	VO2
11111	0.95V	1.1875V	01111	0.79V	0.9875V
11110	0.94V	1.1750V	01110	0.78V	0.9750V
11101	0.93V	1.1625V	01101	0.77V	0.9625V
11100	0.92V	1.1500V	01100	0.76V	0.9500V
11011	0.91V	1.1375V	01011	0.75V	0.9375V
11010	0.90V	1.1250V	01010	0.74V	0.9250V
11001	0.89V	1.1125V	01001	0.73V	0.9125V
11000	0.88V	1.1000V	01000	0.72V	0.9000V
10111	0.87V	1.0875V	00111	0.71V	0.8875V
10110	0.86V	1.0750V	00110	0.70V	0.8750V
10101	0.85V	1.0625V	00101	0.69V	0.8625V
10100	0.84V	1.0500V	00100	0.68V	0.8500V
10011	0.83V	1.0375V	00011	0.67V	0.8375V
10010	0.82V	1.0250V	00010	0.66V	0.8250V
10001	0.81V	1.0125V	00001	0.65V	0.8125V
10000	***0.80V***	***1.0000V***	00000	0.64V	0.8000V

Voltage Control of LDO2, and LDO3

ADDR	Data Bit	Data Name	Function Description
0x14 0x19	b7~b4 b3~b0	VOLDOx _NRM[3:0] /VOLDOx _SLP[3:0]	Setting the output voltage of LDO2, and LDO3 VOLDO2_NRM/VOLDO2_SLP Default=4'b1010 VOLDO3_NRM/VOLDO3_SLP Default=4'b0010

VOLDOx_[3:0]	LDOx	VOLDOx_[3:0]	LDOx	VOLDOx_[3:0]	LDOx	VOLDOx_[3:0]	LDOx
1111	3.1V	1011	1.9V	0111	1.3V	0011	0.95V
1110	3.0V	***1010***	***1.8V***	0110	1.2V	***0010***	***0.90V***
1101	2.6V	1001	1.6V	0101	1.1V	0001	0.85V
1100	2.5V	1000	1.5V	0100	1.0V	0000	0.80V

ON/OFF Control of DCDC Converters and LDOs

ADDR	Data Bit	Data Name	Function Description
0x05	b7~ b0	ONLDOx ONDCx	DCDC1~DCDC6, and LDO2, LDO3 Enable Signal. ONDCx / ONLDOx: DCDCx, LDOx Status 0: Shutdown ***1***: ***Operation***

Discharge Function of DCDC Converters and LDOs

ADDR	Data Bit	Data Name	Function Description
0x06	b7~ b0	ENDIS_DCx ENDIS_Lx	Enable DCDC and LDO output discharge function during PMIC in shutdown mode. Default=1'b0 DCDC converter still has discharge function during power-off procedure even this bit is written to 0 ENDIS_DCx / ENDIS_Lx: Discharge function 0: Disable ***1***: ***Enable***

Power-Key Function and Timing Control

ADDR	Data Bit	Data Name	Function Description
0x02	b7	LPOFF_TO_DO	Setting PMIC operating mode after it finishes power-off sequence caused by /PWRKEY long pressed with duration longer than $T_{dPWRKEYLPOFF}$. Default=1'b1 LPOFF_TO_DO: 0 = Remain in shutdown mode; ***1*** = ***Re-startup by sequence***
0x02	b6	ENLPOFF	Enable PMIC shutdown when /PWRKEY long pressed with duration longer than $T_{dPWRKEYLPOFF}$ defined by register TIME_LPOFF[1:0]. Default=1'b1 $T>T_{dPWRKEYLPOFF}$: 0 = NO; ***1*** = ***YES***
0x02	b5,b4	TIME_IT [1:0]	TIME_IT[1:0] is used to defined the /PWRKEY rising-edge de-bouncing delay time $T_{dbPWRKEYF}$. When /PWRKEY is toggled high with duration longer than $T_{dbPWRKEYF}$, PMIC enters power-on process and the register /PWRKEY_IT is 1'b1. Default=2'b00 TIME_IT[1:0]: ***00*** = ***128mS***; 01 = 0.5S; 10 = 1.0S; 11 = 1.5S
0x02	b3,b2	TIME_LP [1:0]	TIME_LP[1:0] is used to defined the /PWRKEY long-press delay time $T_{dPWRKEYLP}$. When /PWRKEY is toggled high with duration longer than $T_{dPWRKEYLP}$, the register /PWRKEY_LP is 1'b1. Default=2'b01 TIME_LP[1:0]: 00 = 1.0S; ***01*** = ***2.0S***; 10 = 3.0S; 11 = 4.0S
0x02	b1,b0	TIME_LPOFF [1:0]	TIME_LPOFF[1:0] is used to defined the /PWRKEY long-press delay time $T_{dPWRKEYLPOFF}$. When /PWRKEY is toggled high with duration longer than $T_{dPWRKEYLPOFF}$, PMIC enters power-off process, and the register /PWRKEY_LPOFF is 1'b1. The function of /PWRKEY long-press delay to turn off PMIC can be inactive by writing 0 to the register ENLPOFF. Default=2'b11 TIME_LPOFF[1:0]: 00 = 6.0S; 01 = 7.0S; 10 = 8.0S; ***11*** = ***10.0S***

Fault Status of DCDC Converters and LDOs

ADDR	Data Bit	Data Name	Function Description
0x03	b7~b0	ERRDCX ERRLDOx	Record whether the UVP protection of DCDC1~DCDC6, LDO2~LDO3 ever occurs respectively. ERRDCx, ERRLDOx: 0 = NO; 1 = YES
0x04	b3	RST_ERR	Write 1 to this bit to reset 0x03 to 0.

Version Code of G2227

ADDR	Data Bit	Data Name	Function Description
0x20	b7~b3	CHIP_ID [4:0]	CHIP_ID[4:0] is the identification code of G2227, code=5'b11011
0x20	b2~b0	VERSION [2:0]	VERSION[3:0] is the version code of G2227

FUNCTION DESCRIPTION

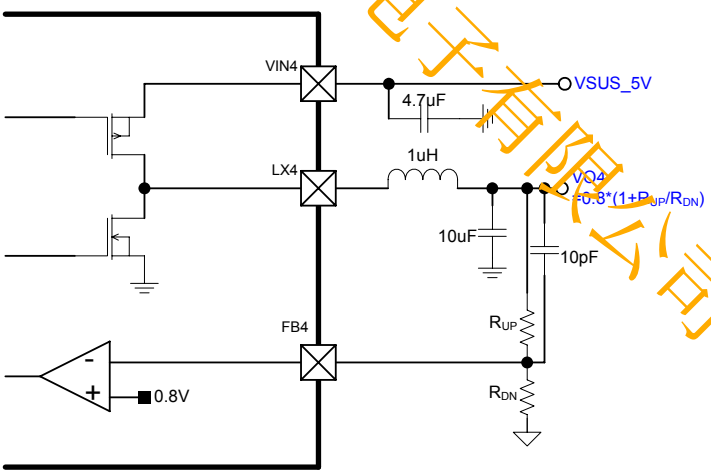
PMU

The G2227 includes six DC/DC Converter, and three LDO regulators to generate a multiple-output power-supply system.

	Topology	Default V_{OUT}	V_{OUT} range	Current rating	ON/OFF Control
DCDC1	3MHz Sync. Buck Converter	3.3V	4-steps voltages from 3.0v to 3.3v configured by I^2C	2.0A	Controlled by register bit ONDC1
DCDC2	3MHz Sync. Buck Converter	1.0V	32-steps DVS from 0.8v to 1.1875v configured by I^2C	3.0A	Controlled by register bit ONDC2
DCDC3	3MHz Sync. Buck Converter	1.0V	32-steps DVS from 0.8v to 1.1875v configured by I^2C	2.0A	Controlled by register bit ONDC3
DCDC4	3MHz Sync. Buck Converter	1.5V	Configured by FB4 pin resistors.	2.0A	Controlled by register bit ONDC4
DCDC5	3MHz Sync. Buck Converter	1.0V	32-steps DVS from 0.8v to 1.1875v configured by I^2C	2.0A	Controlled by register bit ONDC5
DCDC6	3MHz Sync. Buck Converter	1.0V	32-steps DVS from 0.8v to 1.1875v configured by I^2C	2.0A	Controlled by register bit ONDC6
LDO1	RTC LDO	3.1V	4-steps voltages from 3.0v to 3.3v configured by I^2C	50mA	Always ON
LDO2	pMOS LDO	1.8V	16-steps voltages from 0.8v to 3.1v configured by I^2C	600mA	Controlled by register bit ONLDO2
LDO3	pMOS LDO	0.9V	16-steps voltages from 0.8v to 3.1v configured by I^2C	600mA	Controlled by register bit ONLDO3

DCDC4 Output Voltage Setting

The output voltage of DCDC4 is decided according to the resistor R_{UP} connecting between FB4 to converter's output voltage, and the resistor R_{DN} connecting between FB4 to ground. The suggesting resistance of R_{DN} is 160kΩ.



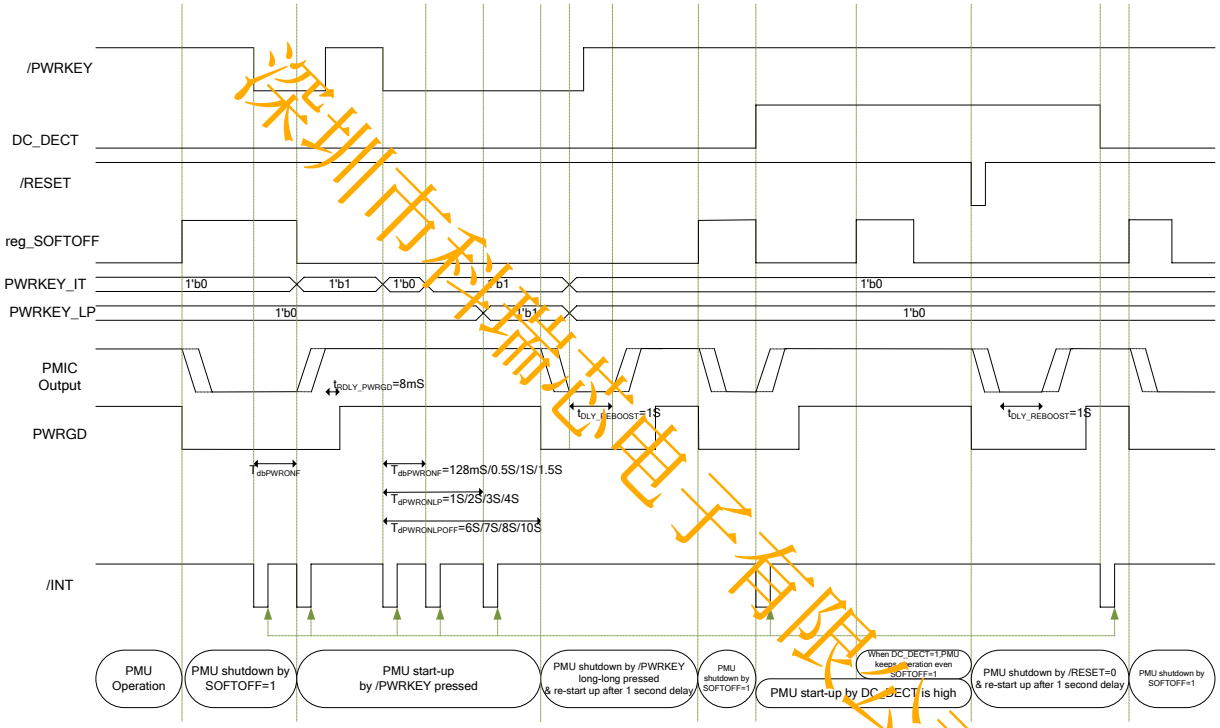
PMU Power ON/OFF Initiation

The following conditions are available to turn on the PMU of G2227:

- /PWRKEY is low-level pressed with duration longer than $T_{dbPWRKEYF}$
- After 1 second delay from shutdown of G2227 caused by /PWRKEY is long-long pressed with duration longer than $T_{dPWRKEYLPOFF,}$ and register ENLPOFF=1'b1, LPOFF_TO_DO=1'b1.
- After 1 second delay from shutdown of G2227 caused by toggling /RESET low.
- The voltage applied in DC_DECT pin is higher than V_{DCDET} (1.2V typ.)
- The voltage applied in VCC pin is higher than V_{VCC_UVLO}+V_{VCC_UVLOHY} (2.8V typ.)

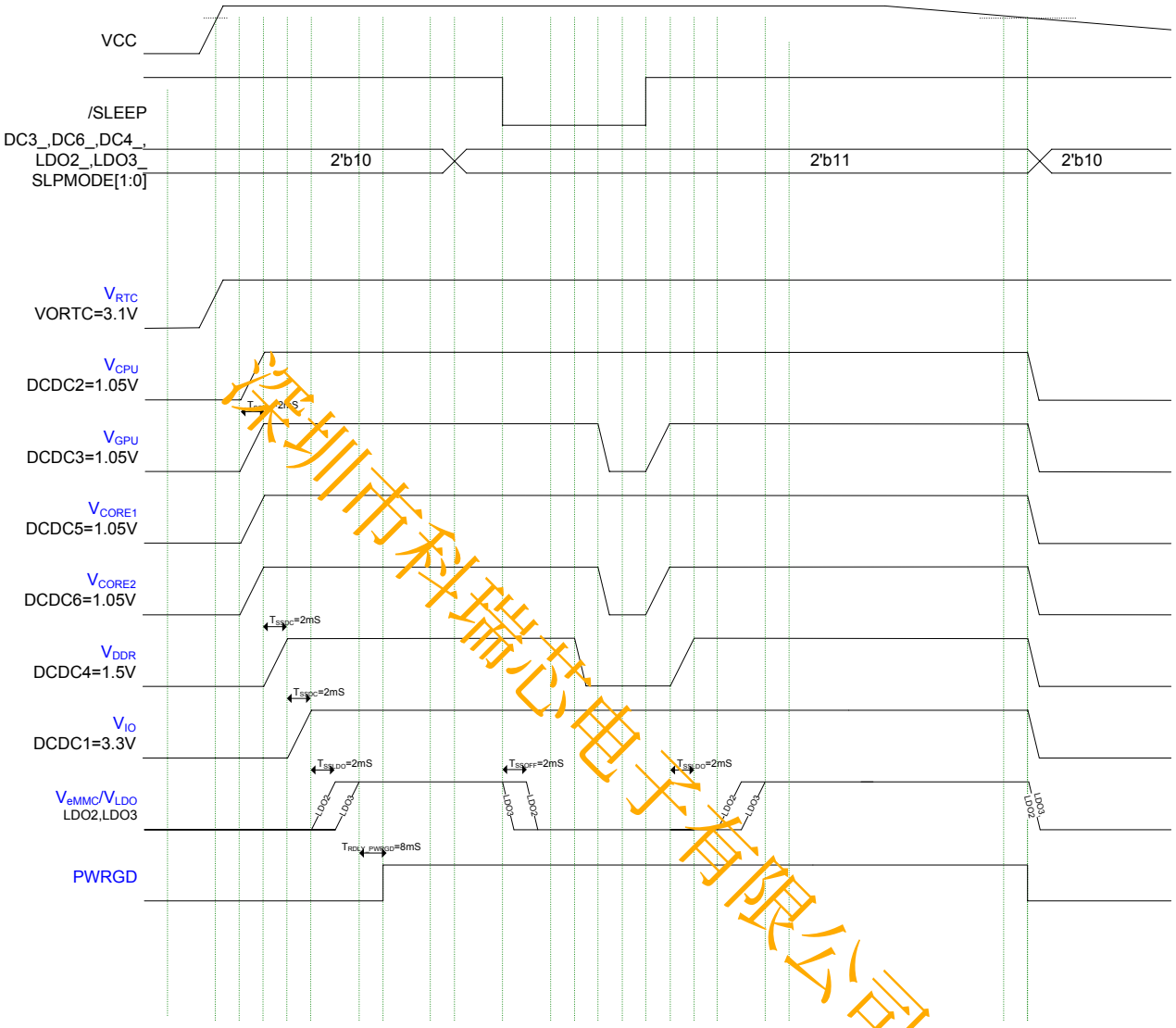
The following conditions are available to turn off the PMU of G2227:

- /PWRKEY low-level pressed with duration longer than $T_{dPWRKEYLPOFF}$ (if ENLPOFF=1'b1)
- Write 1 to register SOFTOFF after PWRGD is turned high and DC_DET is low.
- /RESET is toggle low.
- Output voltage UVP of DCDC converters occurs with duration longer than 128mS
- G2227 thermal shutdown occurs.



PMU Power ON/OFF Sequence

When the power on condition is met, these six DC/DC converters, LDO2, and LDO3 start up in sequence. After these converters finish power on sequence, the open-drain output PWRGD is high with 8ms time delay from LDO3 is power ready. When G2227 enter sleep mode controlled by toggling /SLEEP pin low, PWRGD pin keeps high, and all converters' on/off mode is according to the setting of SLPMODE[1:0] .



PMU Fault Protection

G2227 PMU provides VCC over voltage protection, over-current protection, under-voltage protection, short-circuit protection, and thermal shutdown protection to achieve complete protection.

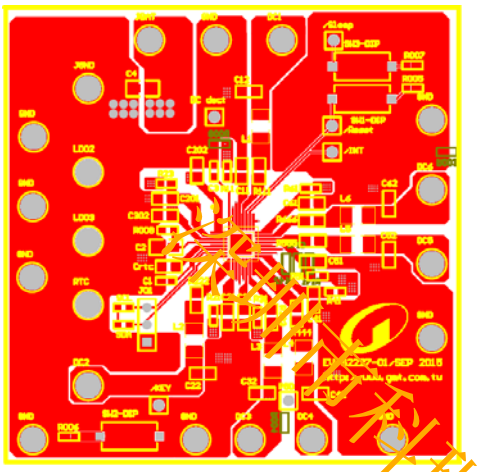
	Protection type	Threshold	Protection methods	Reset Method
VCC	OVP	VCC>5.8V	IC shutdown	Reset by toggling EN_MAIN
DCDC1 Buck	Current Limit	pMOS current>2.5A	pMOS Off, nMOS on	Automatic Reset at next cycle
	UVP	VOUT1<75%*$VOUT_{SET}$	IC shutdown if period above 128ms	Reset by the power- on/off initiation conditions
DCDC2 Buck	Current Limit	pMOS current>3.5A	pMOS Off, nMOS on	Automatic Reset at next cycle
	UVP	VOUT2< $VOUT_{SET}$-100mV	IC shutdown if period above 128ms	Reset by the power- on/off initiation conditions
DCDC3 Buck	Current Limit	pMOS current>2.5A	pMOS Off, nMOS on	Automatic Reset at next cycle
	UVP	VOUT3< $VOUT_{SET}$-100mV	IC shutdown if period above 128ms	Reset by the power- on/off initiation conditions
DCDC4 Buck	Current Limit	pMOS current>2.5A	pMOS Off, nMOS on	Automatic Reset at next cycle
	UVP	VOUT4<90%*$VOUT_{SET}$	IC shutdown if period above 128ms	Reset by the power- on/off initiation conditions
DCDC5 Buck	Current Limit	pMOS current>2.5A	pMOS Off, nMOS on	Automatic Reset at next cycle
	UVP	VOUT5< $VOUT_{SET}$-100mV	IC shutdown if period above 128ms	Reset by the power- on/off initiation conditions
DCDC6 Buck	Current Limit	pMOS current>2.5A	pMOS Off, nMOS on	Automatic Reset at next cycle
	UVP	VOUT6< $VOUT_{SET}$-100mV	IC shutdown if period above 128ms	Reset by the power- on/off initiation conditions
LDO2/3 LDO	Current Limit	pMOS current>600mA		PMOS current<450mA
	UVP	VOUTX<12.5%*$VOUTX_{SET}$	pMOS Off	Reset by the power- on/off initiation conditions, or I^2C ONLDO control
Thermal	TSD	Junction Temp. >150°C	IC shutdown	Reset by the power- on/off initiation conditions

Layout guidelines

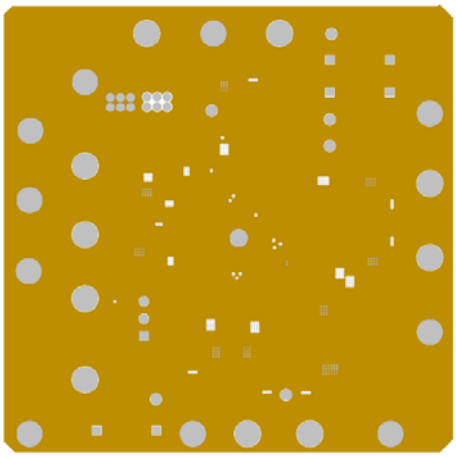
Careful printed circuit layout is extremely important to avoid causing parasitical capacitance and line inductance. The following layout guidelines are recommended to achieve optimum performance.

- Please the buck converter inductor close to the LX pin. Keep traces short, direct, and wide.
- Please ceramic bypass capacitors near the input/output pin.
- All feedback signal must first go through the regulator capacitors. Place feedback connection points near the output capacitors and minimize the control feedback loop as much as possible to achieve the best regulation performance.

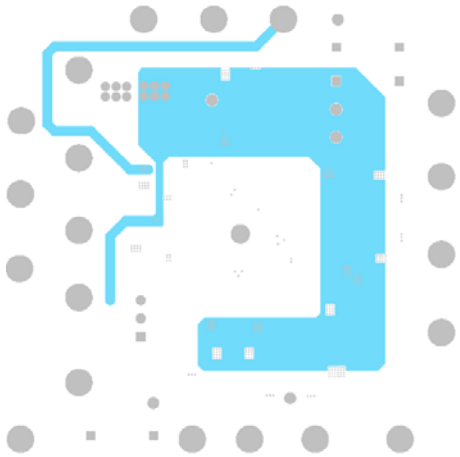
Top Layer



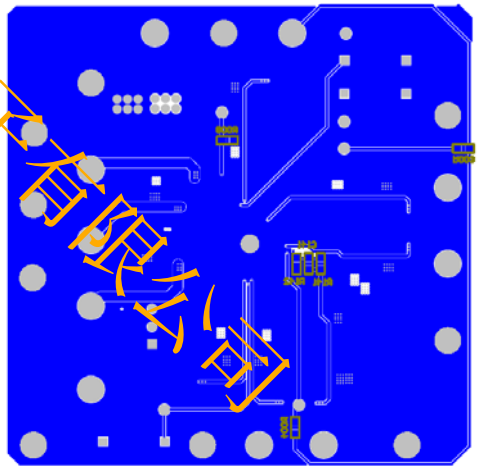
Mid-Layer 1(GND Plane)



Mid-Layer 2

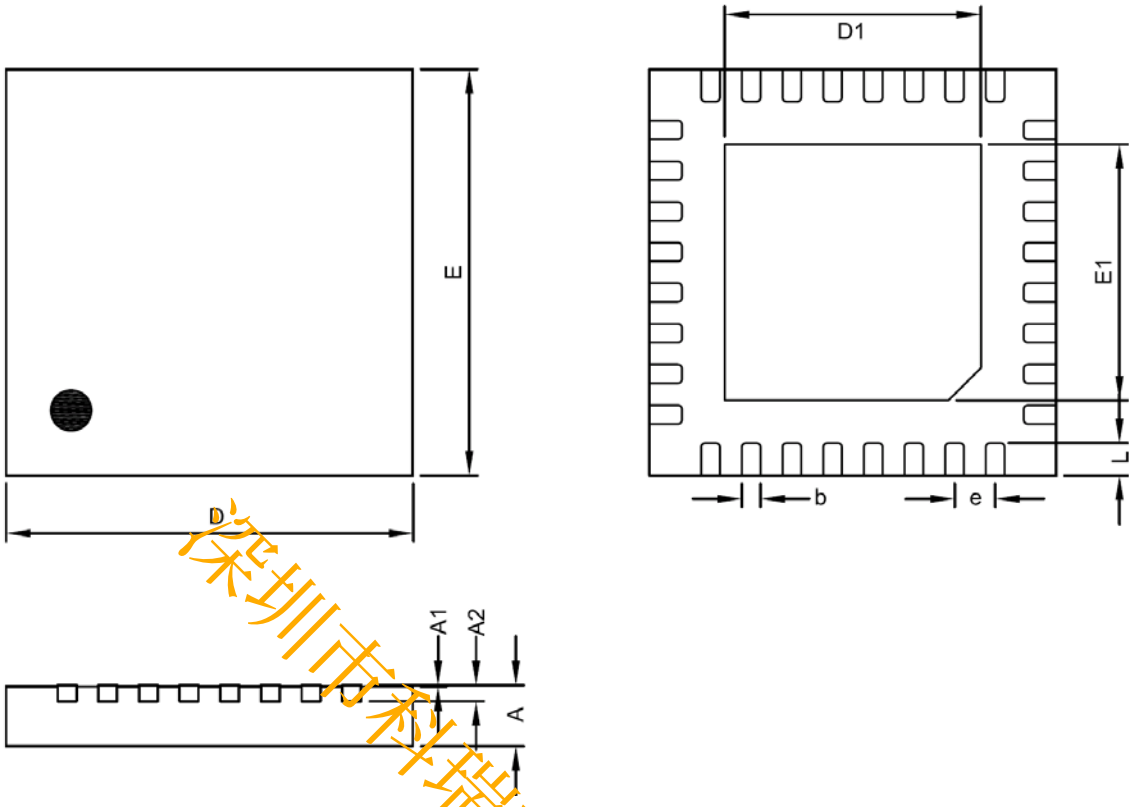


Bottom Layer



EV2227 PCB	Information
Board Material	FR4
Size	66mm×66mm
Board Thickness	1.6mm
Layers	4
Copper Thickness	2 oz.

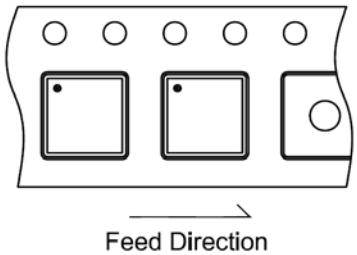
Package Information



TQFN5X5-32 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0.00	---	0.05	0.0000	---	0.0020
A2	0.19	0.20	0.21	0.0075	0.0079	0.0083
D	4.95	5.00	5.05	0.1949	0.1969	0.1988
E	4.95	5.00	5.05	0.1949	0.1969	0.1988
D1	3.05	3.15	3.25	0.1201	0.1240	0.1280
E1	3.05	3.15	3.25	0.1201	0.1240	0.1280
b	0.18	0.23	0.28	0.0071	0.0091	0.0110
e	0.50 BSC			0.0197 BSC		
L	0.35	0.40	0.45	0.0138	0.0157	0.0177

Taping Specification



PACKAGE	Q'TY/REEL
TQFN5X5-32	3,000 ea