I²C Programmable EL Power for OLED

Features

- **Input Voltage Range: 10V to 25V**
- **Two Phase Synchronous Buck Controller for ELVDD**
  - **2V to 8.375V Programmable Output**
  - **6A Current Limit for Single Buck Controller**
- **Two Phase Synchronous Inverting Buck-Boost Controller for ELVSS**
  - **-4V to -18V Programmable Output**
  - **6A Output Current Limit for Single Buck-Boost Controller**
- **Output Discharged Function During Power Down**
- **Adjustable Internal Frequency by external resistor**
- **Externally Adjustable Soft-Start**
- **Adjustable Current Limit**
- **Synchronous to External Clock**
- **500kHz to 1.5MHz Internal Switching Frequency**
- **Spread Spectrum Function**
- **EN Control**
- **Fault Indication Through the PG pin and I²C**
- **Protection Function**
  - **VIN Under Voltage Lock Out (UVLO)**
  - **SCP/UVP/OVP on ELVDD and ELVSS**
  - **Over Current on ELVDD and ELVSS**
  - **Thermal Shut Down (TSD)**
- **AEC-Q100 Grade2 Qualified**
- **-40℃ to 105℃ Operating Temperature Range**
- **Available in TQFN6X6-48 Package**

General Description

The GQ2704A is a complete EL power for large size OLED panel for nowadays automotive application. It includes a two-phase buck controller and a two-phase inverting buck-boost controller.

The GQ2704A is intended to operate with 6.5V to 25V supplies, the ELVDD and ELVSS soft-start time by external capacitor setting, output setting by I2 interface. The ELVDD and ELVSS controller has an internal switching frequency and external clock option. Besides, the GQ2704A built in SCP、UVP、over current、OVP and OTP. If output occurs any protection, the PG pulled low.

The GQ2704A is available in a 48-pin TQFN package and operates in -40°C to +105°C temperature range.

Applications

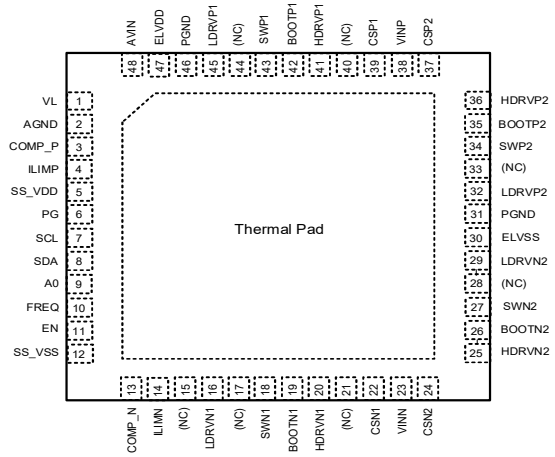
- **Automotive OLED Panel**
- **MNT OLED**

Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
GQ2704ARP1U-K	2704A	-40°C to 105°C	TQFN6X6-48

Note: RP: TQFN6X6-48
1: Bonding Code
U: Tape & Reel
Green : Lead Free / Halogen Free.

Pin Configurations



GQ2704A TQFN6X6-48

Note: Recommend connecting the Thermal Pad to the Ground for excellent power dissipation

Absolute Maximum Ratings

AVIN, VINN, VINP to PGND . . . . . -0.3V to 29V
CSN1, CSN2 to AGND . . . . . -0.3V to 29V
CSP1, CSP2 to AGND . . . . . -0.3V to 29V
BOOTN1, BOOTN2 to SWN1, SWN2 . . . . . -0.3V to 6V
BOOTP1, BOOTP2 to SWN1, SWN2 . . . . . -0.3V to 6V
SWN1, SWN2 to PGND . . . . . -12V to 29V
SWP1, SWP2 to PGND . . . . . .-0.3V to 29V
HDRVP1 to SWP1 . . . . . -0.3V to (BOOTP1+0.3)V
HDRVP2 to SWP2 . . . . . -0.3V to (BOOTP2+0.3)V
HDRVN1, HDRVN2 to PGND . ... -12V to (ELVSS+6)V
HDRVP1, HDRVP2 to PGND . . . . . -0.3V to (VL+0.3)V
ILIMN, ILIMP to AGND . . . . . -0.3V to (VL+0.3)V
SS_VSS, SS_VDD to AGND . . . . -0.3V to (VL+0.3)V
COMP_N, COMP_P to AGND . . . -0.3V to (VL+0.3)V
SDA, SCL to AGND . . . . . .-0.3V to (VL+0.3)V
A0, EN, FREQ to AGND . . . . . -0.3V to (VL+0.3)V
PG to AGND . . . . . -0.3V to (VL+0.3)V
VL to AGND . . . . . .-0.3V to 6V
ELVDD to AGND . . . . . .-0.3V to 29V
ELVSS to AGND . . . . . .-12V to 0.3V
ESD susceptibility:
HBM (Human Body Mode) 2kV

Recommend Operating Range

Thermal Resistance Junction to Ambient, (θ_{JA})
TQFN6X6-48 . . . . . 27.2℃//W
Thermal Resistance Junction to Case, (θ_{JC})
TQFN6X6-48 . . . . . 5.4℃//W
Continuous Power Dissipation (T_A = +25°C)
TQFN6X6-48 . . . . . 3.67W
Operating Temperature . . . . . -40°C to 105°C
Junction Temperature . . . . . 150°C
Storage Temperature . . . . . -65°C to 150°C
Reflow Temperature (soldering, 10 sec) . . . . . 260°C

Electrical Characteristics

(V_{IN}=12V, V_{EN}=3.3V, V_{ELVDD}=5V, V_{ELVSS}=-4V, T_A = 25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply						
VIN Range			10	12	25	V
VIN UVLO Threshold		V_{IN} falling	6.0	6.1	6.2	V
		V_{IN} hysteresis	0.1	0.2	0.3	
AVIN Shutdown Current		EN=GND, AVIN=25V	---	5	---	mA
VIN Quiescent Current		EN=3.3V, VIN=20V, No switching	---	30	---	mA
Internal Regulator						
VL Output Voltage			4.9	5	5.1	V
Thermal Protection						
Thermal Shutdown			---	140	---	°C
Thermal Shutdown Hysteresis			---	20	---	°C
Oscillator Frequency						
Internal Frequency		R_{FREQ}=300 kΩ	425	500	575	KHz
		R_{FREQ}=80 kΩ	1275	1500	1725	KHz
External Frequency Range		2 times external clock	1000	---	3000	KHz
ELVDD Buck Controller						
Output Voltage Range	V_{ELVDD}	Programmable	2	---	8.375	V
Output Voltage Bit			---	8	---	Bits
Output Voltage Resolution			---	0.05	---	V
Output Voltage Accuracy		ELVDD = 4V to 8.375V	-1	---	+1	%
		ELVDD = 2V to 4V	-2.5	---	+2.5	%
Soft-Start Internal Charging Current	T_{SS}	ELVDD=4.5V	---	4.4	---	μA
Maximum Duty Cycle	D_{MAX}		85	90	---	%
Minimum On-Time			---	100	---	ns

Electrical Characteristics (Continued)

(V_{IN}=12V, V_{EN}=3.3V, ELVDD=5V, ELVSS=-9V, T_A = 25°C)

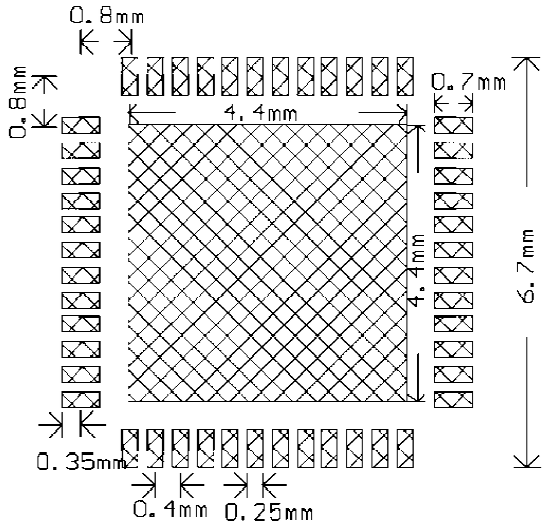
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
High Side Gate Driver		Source=1A	---	1.5	---	Ω
		Sink=1A	---	1.5	---	Ω
Low Side Gate Driver		Source=1A	---	1.5	---	Ω
		Sink=1A	---	1.5	---	Ω
Dead Time			---	20	---	ns
Discharge Resistance		0x00[5]=0	---	4	---	kΩ
		0x00[5]=1	---	0.1	---	kΩ
ELVSS Buck/Boost Inverting Controller						
Output Voltage Range	V_{ELVSS}	Programmable	-4	---	-18	V
Output Voltage Bit			---	8	---	Bits
Output Voltage Resolution			---	0.1	---	V
Output Voltage Accuracy			-1	---	+1	%
Soft-Start Internal Charging Current	T_{SS}	ELVSS=-9V	---	2.1	---	μA
Maximum Duty Cycle	D_{MAX}		85	90	---	%
Minimum On-Time			---	100	---	ns
High Side Gate Driver		Source=1A	---	1.5	---	Ω
		Sink=1A	---	1.5	---	Ω
Low Side Gate Driver		Source=1A	---	1.5	---	Ω
		Sink=1A	---	1.5	---	Ω
Dead Time			---	20	---	ns
Fault Protection						
ELVDD Under-voltage Fault Threshold		ELVDD falling	60	70	80	%
ELVSS Under-voltage Fault Threshold		ELVSS rising	60	70	80	%
Under-voltage Fault Timer		After Delay time , PG pull low	4	5	6	ms
ELVDD Short-Circuit Fault Threshold		ELVDD falling	10	20	30	%
ELVSS Short-Circuit Fault Threshold		ELVSS rising	10	20	30	%
Short-Circuit Fault Timer		After Delay time , PG pull low	200	250	300	μs
ELVDD Over-Current Fault Timer			---	10	---	ms
ELVSS Over-Current Fault Timer			---	10	---	ms
ELVDD Over- voltage Fault Threshold		ELVDD =5V	---	120	---	%
ELVSS Over- voltage Fault Threshold		ELVSS =-9V	---	120	---	%
OVP Hysteresis			---	TBD	---	V
Comp Maximum Voltage			---	3.5	---	V
Comp Fault Timer		After Delay time , PG pull low	---	2	---	s
ELVSS Leakage Current Fault Threshold			---	0.2	---	V
Discharge Resistance		0x00[5]=0	---	1.2	---	kΩ
		0x00[5]=1	---	0.1	---	kΩ
Logic Input(EN,A0,FREQ)						
Input Logic High			1.2	---	---	V
Input Logic Low			---	---	0.4	V
EN ,A0 Pull down Resistor			---	100	---	kΩ

I²C Timing Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I2C compatible Interface (SCL, SDA)						
High-level Input Voltage	V_{IH}		1.2	---	---	V
Low-level Input Voltage	V_{IL}		---	---	0.4	V
SDA, SCL input current	I_{in}		-2	0	2	μA
SCL Frequency	F_{CLK}		---	---	400	kHz
SCL High Period	T_{HIGH}		0.3	---	---	μs
SCL Low Period	T_{LOW}		0.4	---	---	μs
SCL Rise Time	T_r		---	---	0.3	μs
SCL Fall Time	T_f		---	---	0.3	μs
Start Condition Hold Time			0.25	---	---	μs
Start Condition Setup Time			0.25	---	---	μs
SDA Hold Time			50	---	---	ns
SDA Setup time			50	---	---	ns
ACK Delay Time			---	---	0.35	μs
ACK Hold Time			---	0.1	---	μs
Stop Condition Setup Time			0.25	---	---	μs
Bus Free Time			0.5	---	---	μs
Bus Capacitance			---	---	400	pF
Spike Rejection Pulse Width			---	0.05	---	μs

Minimum Footprint PCB Layout Section

TQFN6X6-48



Pin Description

Pin No.	Pin Name	Pin Description
1	VL	Internal regulator output
2	AGND	Analog ground connection
3	COMP_P	ELVDD compensation node. Connect external compensation elements to this pin to stabilize the control loop.
4	ILIMP	ELVDD current limit setup pin. Connect a resistor from this pin to ground to set the current limit value.
5	SS_VDD	ELVDD soft-start programming pin. Connect an external capacitor between this pin and ground to set the soft-start time.
6	PG	Open-drain power-good indication output. PG will be pulled low to ground if any internal protection is triggered.
7	SCL	I²C interface clock
8	SDA	I²C interface data
9	A0	I²C address-selection pin
10	FREQ	Resistor-programmable switching frequency setting control input. Connect a resistor from FREQ to AGND to set the internal switching frequency.
11	EN	Enable control input. A logic-high enables the converter; a logic-low forces the device into shutdown mode.
12	SS_VSS	ELVSS soft-start programming pin. Connect an external capacitor between this pin and ground to set the soft-start time.
13	COMP_N	ELVSS compensation node. Connect external compensation elements to this pin to stabilize the control loop.
14	ILIMN	ELVSS current limit setup pin. Connect a resistor from this pin to ground to set the current limit value.
15,17,21,28 33,40,44	NC	No internal connection
16	LDRVN1	ELVSS low-side gate driver output for single phase 1. Connect this pin to the gate of low-side MOSFET.
18	SWN1	ELVSS switch node for single phase 1. Connect this pin to the source of high-side MOSFET and the drain of the low-side MOSFET.
19	BOOTN1	ELVSS single phase 1 high-side driver supply for bootstrap gate drive.
20	HDRVN1	High side gate driver output for ELVSS single phase 1. Connect this pin to the gate of high-side MOSFET.
22	CSN1	Current sense amplifier input for ELVSS single phase1.
23	VINN	ELVSS power input and current sense amplifier input. Connect current sense resistor to the input power for ELVSS single phase 1&2.
24	CSN2	Current sense amplifier input for ELVSS single phase2.
25	HDRVN2	High side gate driver output for ELVSS single phase 2. Connect this pin to the gate of high-side MOSFET.
26	BOOTN2	ELVSS single phase 2 high-side driver supply for bootstrap gate drive.
27	SWN2	ELVSS switch node for single phase 2. Connect this pin to the source of high-side MOSFET and the drain of the low-side MOSFET.
29	LDRVN2	ELVSS low-side gate driver output for single phase 2. Connect this pin to the gate of low-side MOSFET.
30	ELVSS	ELVSS regulator output.

Pin Description (Continued)

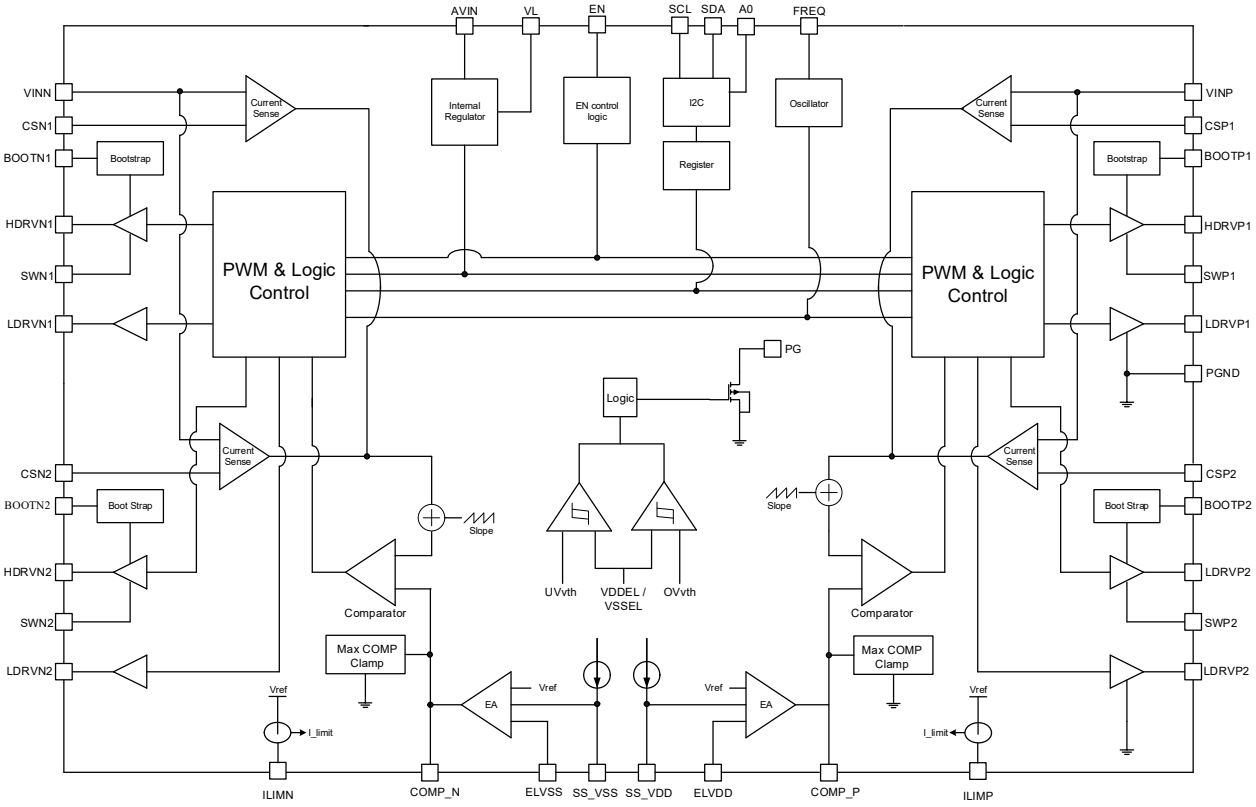
Pin No.	Pin Name	Pin Description
31,46	PGND	Power GND
32	LDRVP2	ELVDD low-side gate driver output for single phase 2. Connect this pin to the gate of low-side MOSFET.
34	SWP2	ELVDD switch node for single phase 2. Connect this pin to the source of high-side MOSFET and the drain of the low-side MOSFET.
35	BOOTP2	ELVDD single phase 2 high-side driver supply for bootstrap gate drive.
36	HDRVP2	High side gate driver output for ELVDD single phase 2. Connect this pin to the gate of high-side MOSFET.
37	CSP2	Current sense amplifier input for ELVDD single phase2.
38	VINP	ELVDD power input and current sense amplifier input. Connect current sense resistor to the input power for ELVDD single phase 1&2
39	CSP1	Current sense amplifier input for ELVDD single phase1.
41	HDRVP1	High side gate driver output for ELVDD single phase 1. Connect this pin to the gate of high-side MOSFET.
42	BOOTP1	ELVDD single phase 1 high-side driver supply for bootstrap gate drive.
43	SWP1	ELVDD switch node for single phase 1. Connect this pin to the source of high-side MOSFET and the drain of the low-side MOSFET.
45	LDRVP1	ELVDD low-side gate driver output for single phase 1. Connect this pin to the gate of low-side MOSFET.
47	ELVDD	ELVDD regulator output.
48	AVIN	EL IC power input

Overview

The GQ2704A is a switching buck controller and inverting buck/boost controller. The GQ2704A is configured to provide an adjustable output from 2V to 8.375V for ELVDD and provide an adjustable output from -4V to -18V for ELVSS.

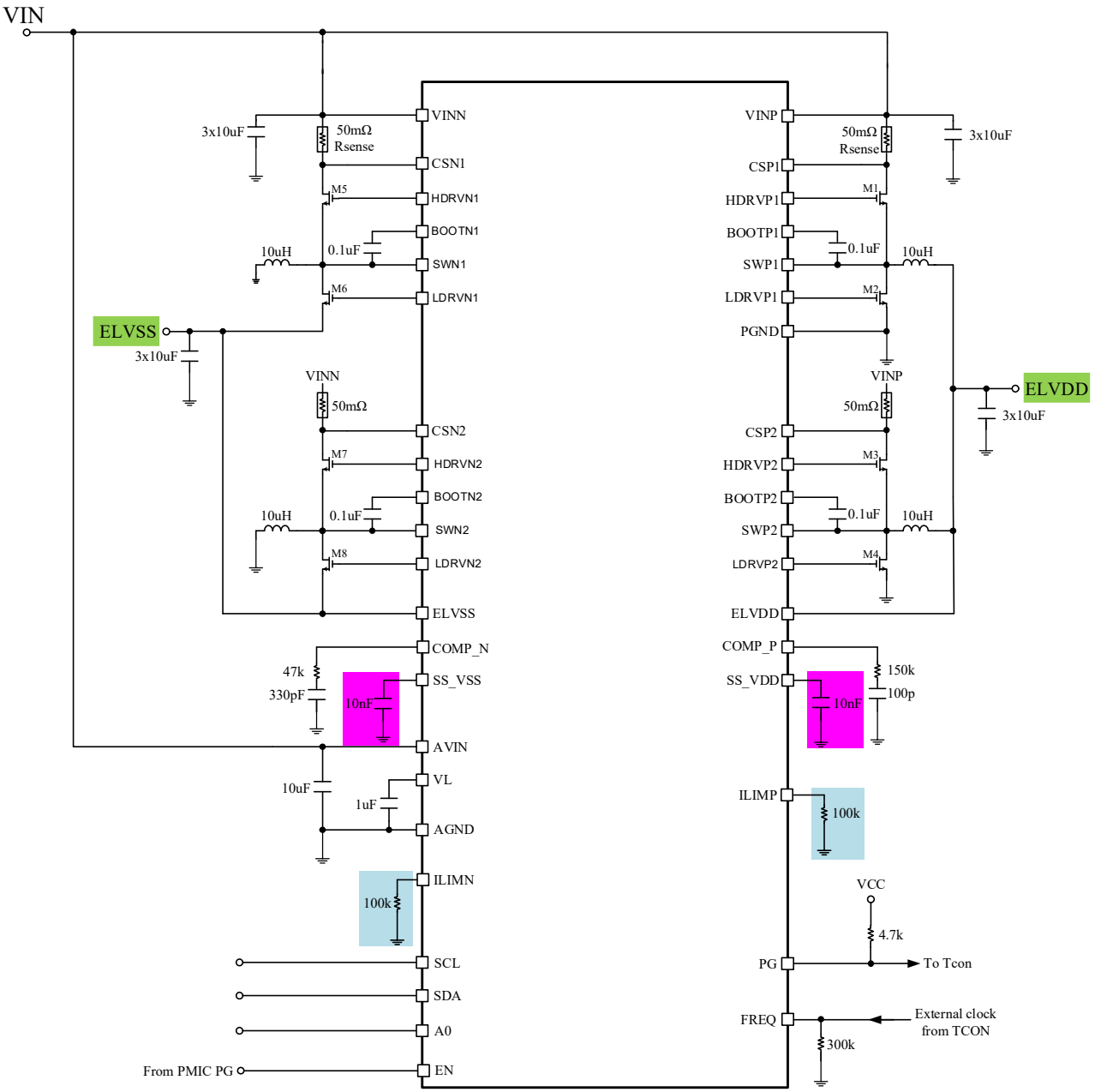
The peak current-mode control using a shunt resistor current sensing provides inherent, cycle-by-cycle peak current limiting, and easy loop compensation. The oscillator frequency is user-programmable between 500 kHz to 1.5 MHz, and the frequency can be synchronized as high as 2 MHz by applying an external clock to the FREQ pin. The fault protection features include current limiting, thermal shutdown, UVLO, and remote shutdown capability. The GQ2704A is provided in a 48-pin TQFN package with exposed pad to aid in thermal dissipation.

Function Block Diagram



Application Circuit

(1) Bipolar OLED application(dual phase)

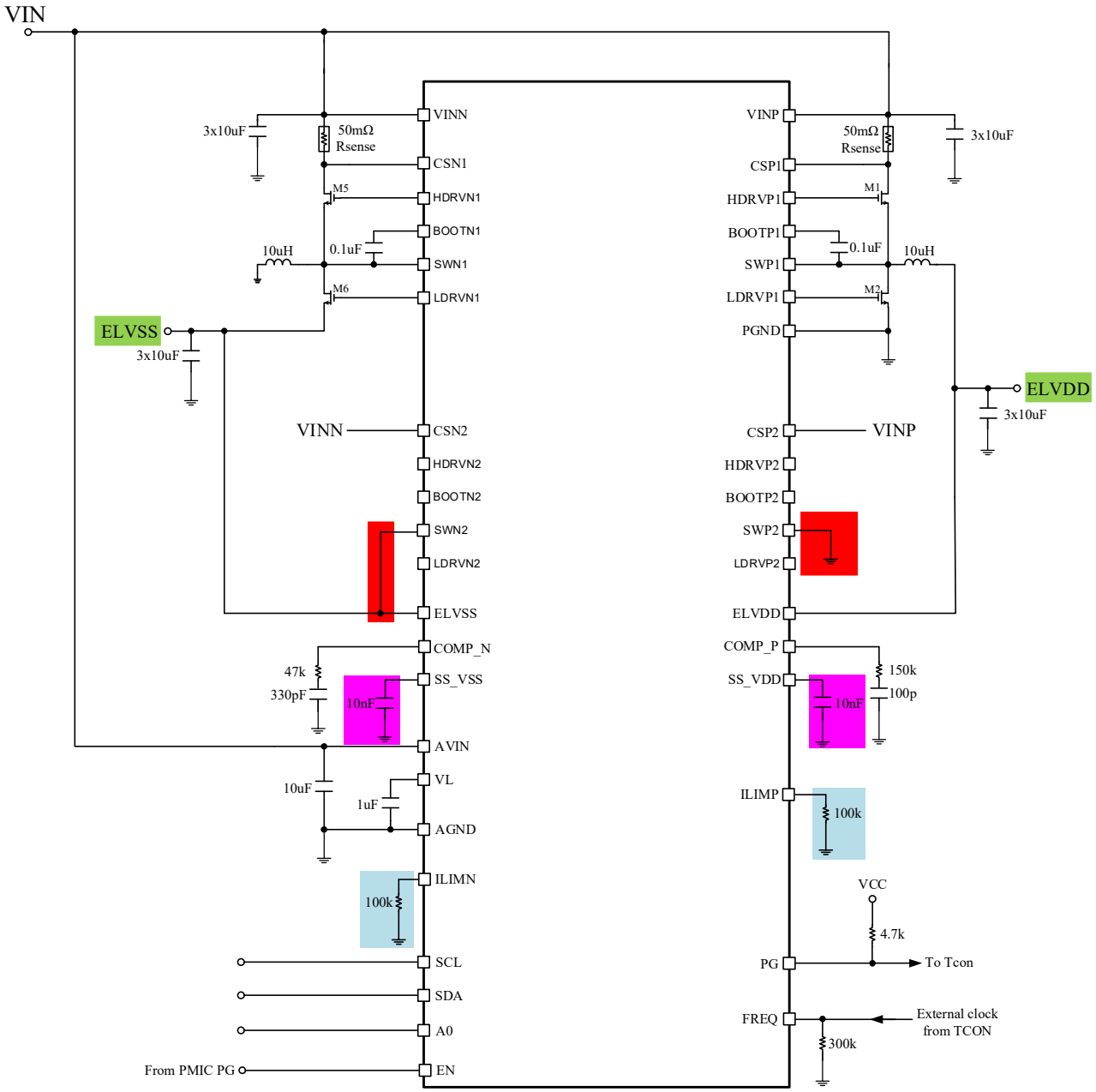


Note:

(1) M1、M2、M3、M4、M5、M6、M7、M8: DMTH6016LPSQ

(2) Rsense VSRP2512S2-R050F

(2) Bipolar OLED application(single phase)



Note:

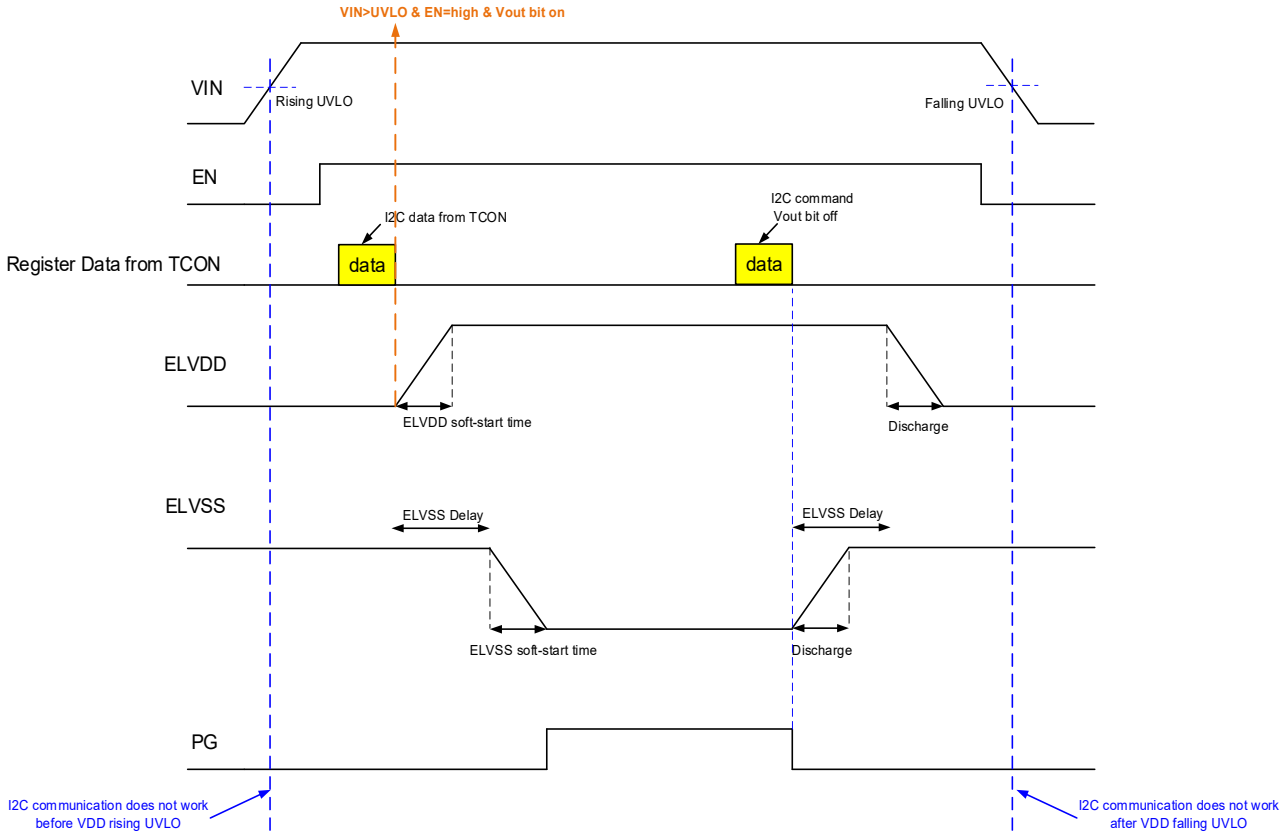
(1) M1、M2、M5、M6: DMTH6016LPSQ

(2) If used to single phase mode, please follow above application circuit

(3) Rsense VSRP2512S2-R050F

Power On/Off Sequence

1. Normal Operation (I²C command vout bit off)

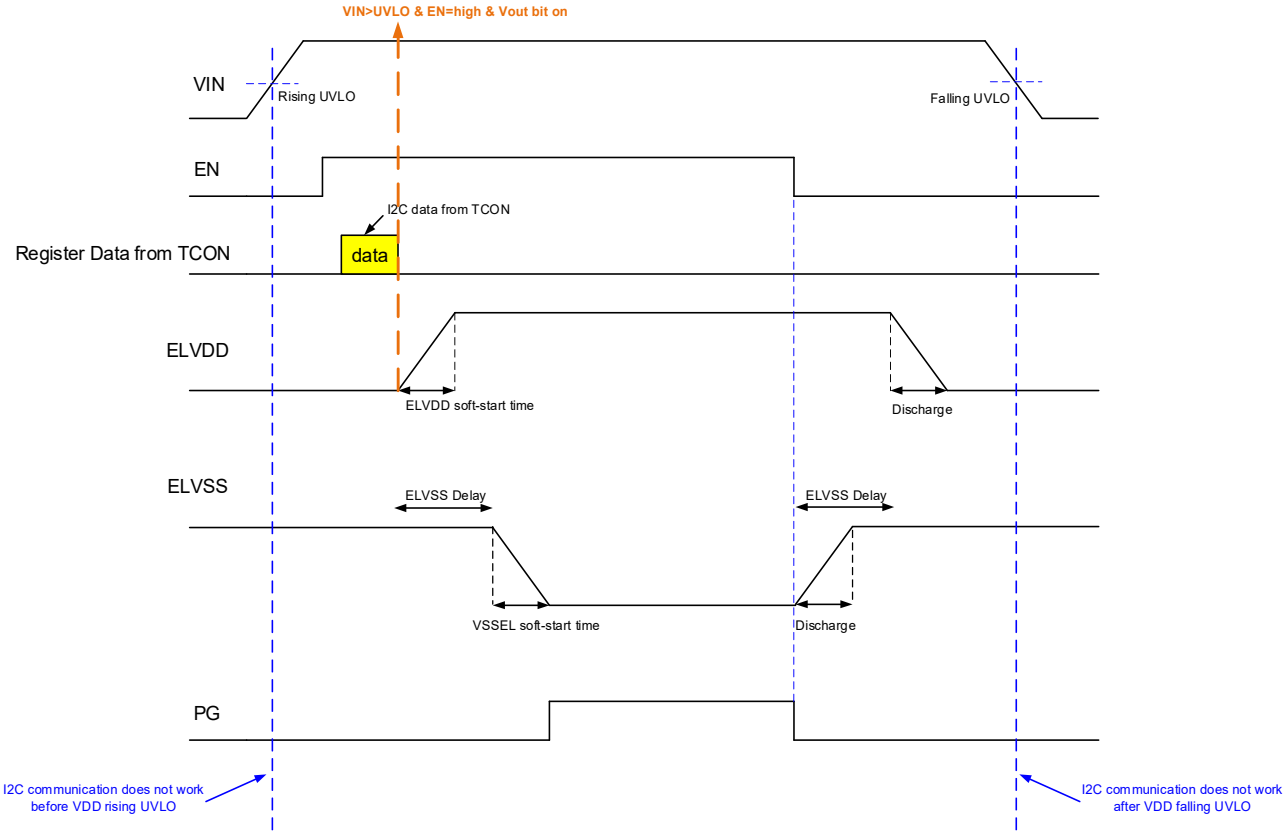


Note:

(1) EN Deglitch time =5ms

(2) A glitch in the EN signal with a period less than 5ms is ignored by the internal enable circuitry.

2. Normal Operation (EN off)

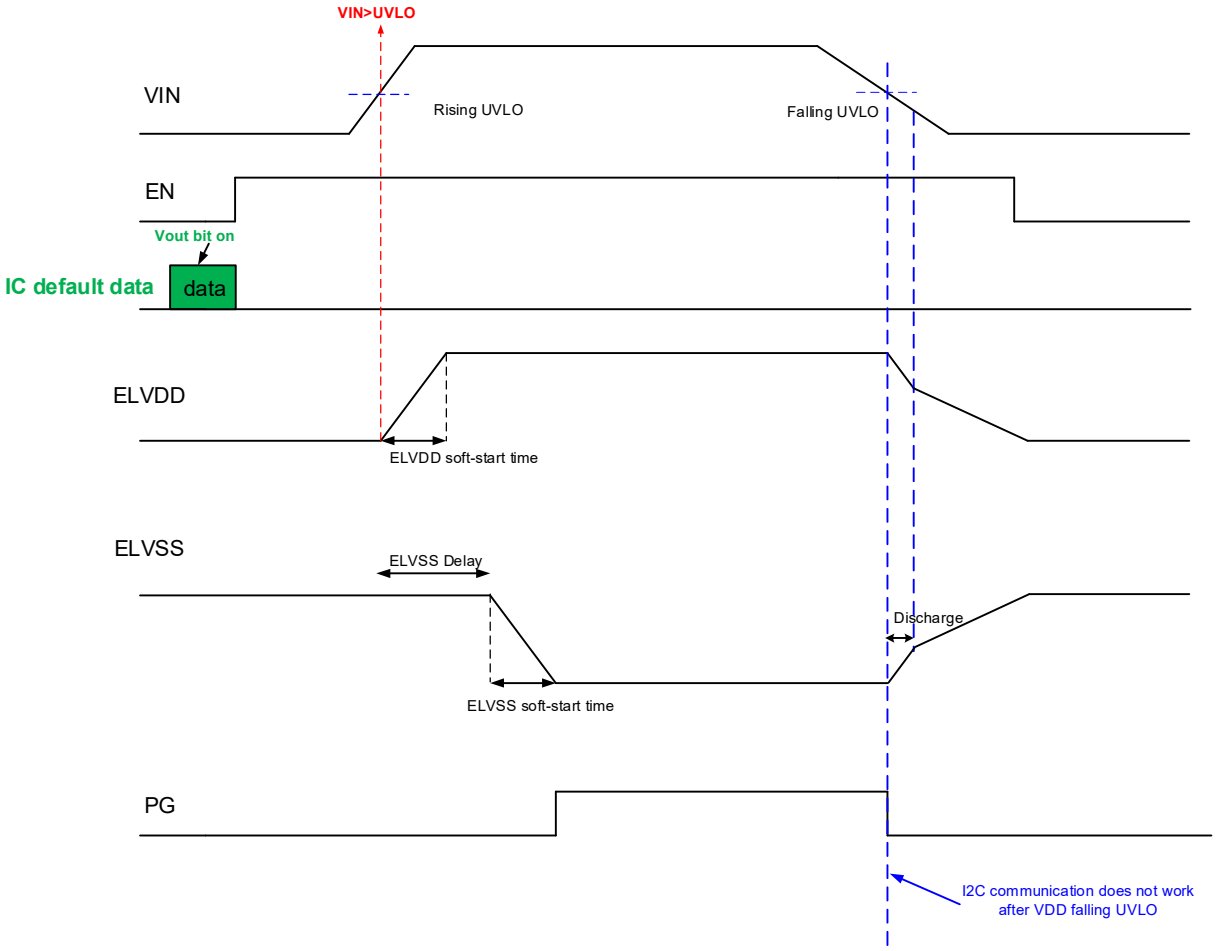


Note:

(1) EN Deglitch time =5ms

(2) A glitch in the EN signal with a period less than 5ms is ignored by the internal enable circuitry.

3. Normal Operation (VIN off)



Note:

(a) EN Deglitch time =5ms

(b) A glitch in the EN signal with a period less than 5ms is ignored by the internal enable circuitry.

Application Information

Soft-Start

The GQ2704A provides adjustable soft-start function. The soft-start function is used to prevent large inrush current while converter is being powered-up. For the GQ2704A the soft-start timing can be programmed by the external capacitor CSS between SS pin and ground. The typical soft start time (Tss) setting value is calculated as follows:

$$SS_{VDD}(ms) = SS_{VSS}(ms) = 0.3 \times CSS(nF)$$

The failure modes and effects analysis (FMEA) consideration are also applied to SS pin setting to avoid abnormal capacitance operation at failure condition. It includes failure scenarios of short-circuit to ground and the pin is left open. The SS time can't set more than 10ms or less than 100us, otherwise it will enter protection.

Inductor Peak Current Limit Setting

The current limit of high side MOSFET switch is adjustable by an external resistor connected to the ILIM pin. Inductor current ripple current also should be considered into current limit setting. The current limit value below offers approximate formula:

$$R_{ILIMP}(k\Omega) = R_{ILIMN}(k\Omega) = \frac{13.3}{(I_{OC} + 0.9) \times Rsense}$$

Where IOC is the desire current limit value (A)

The failure modes and effects analysis (FMEA) consideration are also applied to RLIM pin setting to avoid abnormal current limit operation at failure condition. It includes failure scenarios of short-circuit to ground and the pin is left open. The inductor peak current limit will be 6.5A (typically) when the RLIM pin short to ground and 1.5A (typically) when the RLIM pin is left open. Note that the inductor peak current limit variation increases as the tolerance of RLIM increases. As the RLIM value is small, the inductor peak current limit will probably be operated as RLIM pin short to ground, and vice versa. The RLIM variation range is limited from 30kΩ to 100kΩ to eliminate the undesired inductor peak current limit. When choosing a RLIM other than the recommended range, please make sure that there is no problem by evaluating it with real machine.

Minimum On-Time

The minimum on-time, TON_MIN, is the smallest duration of time in which the high-side MOSFET switch can be in its "on" state. The minimum on-time is 100ns (typically). In continuous mode operation, the minimum on-time limit imposes a maximum operating input voltage. TON must be greater than TON-MIN

For ELVDD:

$$D = \frac{VOUT}{VIN}$$
$$T_{ON} = T \times D = \frac{1}{Fsw} \times D$$
$$T_{OFF} = T \times (1 - D) = \frac{1}{Fsw} \times (1 - D)$$

For ELVSS:

$$D = \frac{VOUT}{VOUT - VIN}$$
$$T_{ON} = T \times D = \frac{1}{Fsw} \times D$$
$$T_{OFF} = T \times (1 - D) = \frac{1}{Fsw} \times (1 - D)$$

Where FSW is the operating frequency.

FCCM Mode

The With a logic high on the 0x01h[1] and 0x01h[0], the device is locked in PWM mode. This operation is maintained, even at no-load, by allowing the inductor current to reverse its normal direction. This mode trades off reduced light load efficiency for low output voltage ripple, tight output voltage regulation, and constant switching frequency. In this mode, a negative current limit of is imposed to prevent damage to the low-side FET of the regulator.

With 0x01h[1] and 0x01h[0] bit is low, the diode emulation feature is activated. Device operation is the same as above; however, the regulator goes into DCM operation when the valley of the inductor current reaches zero. This feature may be activated and deactivated while the part is regulating without removing the load. This feature activates and deactivates gradually.

Spread-Spectrum Function

The spread spectrum is a factory option. In order to find which parts have spread spectrum enabled, The purpose of the spread spectrum is to eliminate peak emissions at specific frequencies by spreading emissions across a wider range of frequencies than a part with fixed frequency operation. Low frequency conducted emissions from the first few harmonics of the switching frequency can be easily filtered. A more difficult design criterion is reduction of emissions at higher harmonics which fall in the FM band. These harmonics often couple to the environment through electric fields around the switch node. The GQ2704A devices use a ±3% or ±6% spread of frequencies which spread energy smoothly across the FM band but is small enough to limit sub-harmonic emissions below its switching frequency.

EN Control

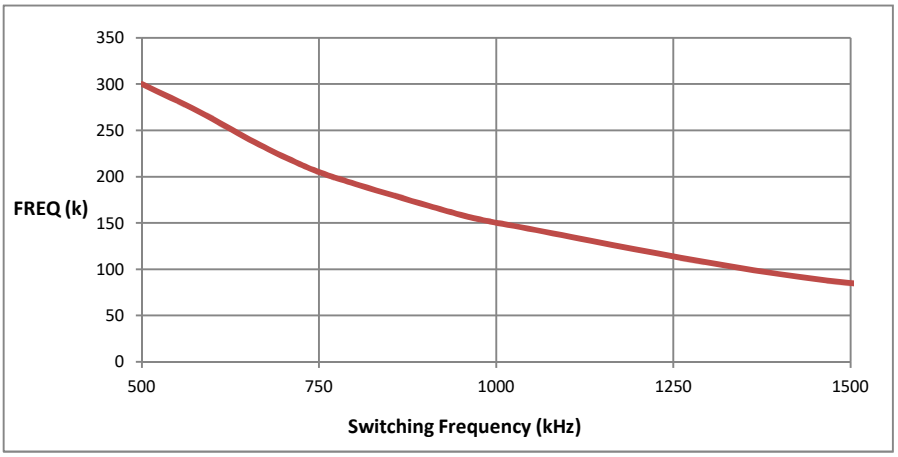
The devices allow for flexible power-up/power-down sequencing and timing of the EL-driver power supplies (ELVDD and ELVSS). Toggling the EN pin from low to high initiates an adjustable preset power-up sequence. Toggling the EN pin from high to low initiates an adjustable preset power-down sequence. The EN pin has an internal deglitch time of 5ms (typ). Figure 11 shows a waveform of the internal EN signal, along with the EN input. Note: A glitch in the EN signal with a period less than 5ms is ignored by the internal enable circuitry.

ELVDD and ELVSS output setting

Care must be taken to follow below regulation to set an accurate and safe output voltage via I^2C setting.

1. VIN must be higher than ELVDD setting voltage a certain level to ensure a correct Buck conversion.
2. Each converter has minimum on time to limit the power conversion rate if VIN voltage keeps high as well as a lower output voltage (absolute value) is set.
3. The voltage difference between VIN and target ELVSS must be less than absolute maximum rating voltage listed, 29V.

FREQ setting Curve



I²C Protocol Definition

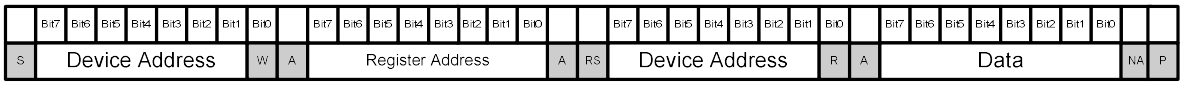
The GQ2704A features an I2C compatible, 2-wire serial interface consisting of a serial-data line (SDA) and a serial-clock line (SCL). SDA and SCL facilitate communication between the GQ2704A and the master at clock rates up to 1MHz. The Master, typically a TCON, generates SCL and initiates data transfer on the bus. The Slave ID of the GQ2704A is chosen by combining the connection of A0 pin to either GND or VCC, as device address table as below.

A0 Pin Connection	Device Address								Write Address	Read Address
	bit7	bit6	bit5	bit4	bit3	Bit2	Bit1(A0)	Bit0(W/R)		
GND	1	0	1	1	1	0	0	0	B8	×
GND	1	0	1	1	1	0	0	1	×	B9
VCC	1	0	1	1	1	0	1	0	BA	×
VCC	1	0	1	1	1	0	1	1	×	BB

Single Mode:

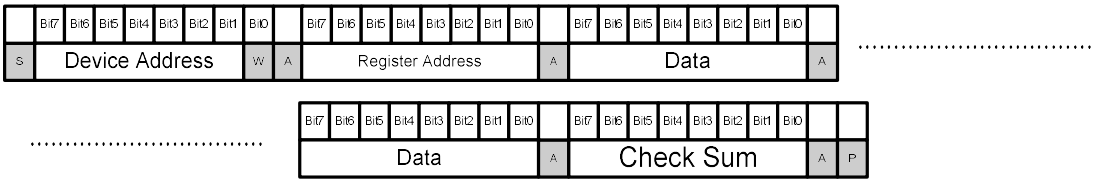
Single Write to DAC register

Single Read to DAC register

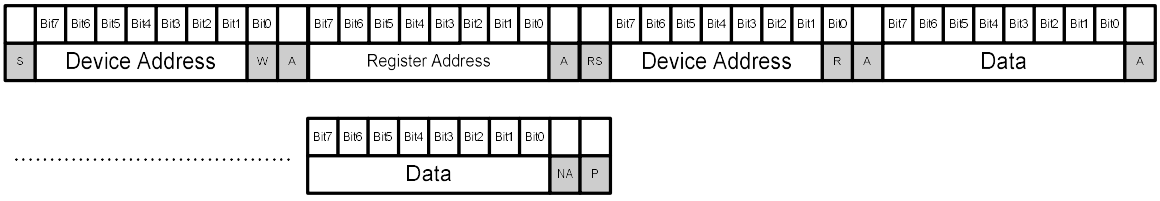


Multi Mode:

Multi Write to DAC registers



Multi Read to DAC register



Note: 1. ID (Device Address) Format

Device Address							
bit7	bit6	bit5	bit4	bit3	Bit2	Bit1	Bit0
1	0	1	1	1	0	A0	R/W
1	0	1	1	1	0	A0	R/W

2. S = start
3. P = stop signal

GQ2704A Register Map

Device Address: 0xB8h

Register	Type	Address	Resolution	Default	MSB	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	LSB
Ctrl1	Read/ Write	00h	8bit	3BH	Spread Spectrum[7:6]		Auto Discharge[5]	Switching Delay[4:3]		Phase Auto[2]	Phase Single/Dual@ ELVSS[1]	Phase Single/Dual@ ELVDD[0]
Ctrl2	Read/ Write	01h	8bit	8FH	Vout [7]	Check Sum[6]	Gate Driver Slew Rate[5:4]		ELVSS Delay from ELVDD [3:2]		ELVSS_FCCM	ELVDD_FCCM
ELVDD Level	Read/ Write	02h	8bit	78H	ELVDD Level [7:0]							
ELVSS Level	Read/ Write	03h	8bit	33H	ELVSS Level [7:0]							
Fault	Read	04h	8bit	00H	Reserved	LCP	COMP	UVP	TSD	OVP	SCP	OCP

Registers and DAC Settings

Spread Spectrum – Address 0x00h [7:6]

DAC Value	Value (%)	DAC Value	Value (%)	DAC Value	Value (%)	DAC Value	Value (%)
00h	off	01h	3	02h	6	03h	-

Auto Discharge – Address 0x00h [5]

DAC Value	Value (Ω)	DAC Value	Value (Ω)
0h	Off	1h	100

Switching Delay – Address 0x00h [4:3]

DAC Value	Delay (ns)	DAC Value	Delay (ns)	DAC Value	Delay (ns)	DAC Value	Delay (ns)
00h	100	01h	150	02h	200	03h	250

Phase Auto – Address 0x00h [2]

DAC Value	Mode	DAC Value	Mode
0h	Phase Manual	1h	Phase Auto

Phase Single/Dual @ELVDD – Address 0x00h [1]

DAC Value	Mode	DAC Value	Mode
0h	Single	1h	Dual

Phase Single/Dual @ELVSS – Address 0x00h [0]

DAC Value	Mode	DAC Value	Mode
0h	Single	1h	Dual

V_{OUT} – Address 0x01h [7]

DAC Value	Status	DAC Value	Status
0h	Off	1h	On

Check Sum – Address 0x01h [6]

DAC Value	Status	DAC Value	Status
0h	Off	1h	On

Gate Driver Slew Rate – Address 0x01h [5:4]

DAC Value	Delay (ns)	DAC Value	Delay (ns)	DAC Value	Delay (ns)	DAC Value	Delay (ns)
00h	Slow	01h	Normal	02h	Fast	03h	Fastest

ELVSS Delay from ELVDD – Address 0x01h [3:2]

DAC Value	Delay (ms)	DAC Value	Delay (ms)	DAC Value	Delay (ms)	DAC Value	Delay (ms)
00h	0	01h	5	02h	10	03h	15

ELVSS FCCM – Address 0x01h [1]

DAC Value	Status	DAC Value	Status
0h	Off	1h	On

ELVDD FCCM – Address 0x01h [0]

DAC Value	Status	DAC Value	Status
0h	Off	1h	On

ELVDD Level – Address 0x02h [7:0]

DAC Value	ELVDD(V)	DAC Value	ELVDD(V)	DAC Value	ELVDD(V)	DAC Value	ELVDD(V)
00	2.000	30	3.200	60	4.400	90	5.600
01	2.025	31	3.225	61	4.425	91	5.625
02	2.050	32	3.250	62	4.450	92	5.650
03	2.075	33	3.275	63	4.475	93	5.675
04	2.100	34	3.300	64	4.500	94	5.700
05	2.125	35	3.325	65	4.525	95	5.725
06	2.150	36	3.350	66	4.550	96	5.750
07	2.175	37	3.375	67	4.575	97	5.775
08	2.200	38	3.400	68	4.600	98	5.800
09	2.225	39	3.425	69	4.625	99	5.825
0A	2.250	3A	3.450	6A	4.650	9A	5.850
0B	2.275	3B	3.475	6B	4.675	9B	5.875
0C	2.300	3C	3.500	6C	4.700	9C	5.900
0D	2.325	3D	3.525	6D	4.725	9D	5.925
0E	2.350	3E	3.550	6E	4.750	9E	5.950
0F	2.375	3F	3.575	6F	4.775	9F	5.975
10	2.400	40	3.600	70	4.800	A0	6.000
11	2.425	41	3.625	71	4.825	A1	6.025
12	2.450	42	3.650	72	4.850	A2	6.050
13	2.475	43	3.675	73	4.875	A3	6.075
14	2.500	44	3.700	74	4.900	A4	6.100
15	2.525	45	3.725	75	4.925	A5	6.125
16	2.550	46	3.750	76	4.950	A6	6.150
17	2.575	47	3.775	77	4.975	A7	6.175
18	2.600	48	3.800	78	5.000	A8	6.200
19	2.625	49	3.825	79	5.025	A9	6.225
1A	2.650	4A	3.850	7A	5.050	AA	6.250
1B	2.675	4B	3.875	7B	5.075	AB	6.275
1C	2.700	4C	3.900	7C	5.100	AC	6.300
1D	2.725	4D	3.925	7D	5.125	AD	6.325
1E	2.750	4E	3.950	7E	5.150	AE	6.350
1F	2.775	4F	3.975	7F	5.175	AF	6.375
20	2.800	50	4.000	80	5.200	B0	6.400
21	2.825	51	4.025	81	5.225	B1	6.425
22	2.850	52	4.050	82	5.250	B2	6.450
23	2.875	53	4.075	83	5.275	B3	6.475
24	2.900	54	4.100	84	5.300	B4	6.500
25	2.925	55	4.125	85	5.325	B5	6.525
26	2.950	56	4.150	86	5.350	B6	6.550
27	2.975	57	4.175	87	5.375	B7	6.575
28	3.000	58	4.200	88	5.400	B8	6.600
29	3.025	59	4.225	89	5.425	B9	6.625
2A	3.050	5A	4.250	8A	5.450	BA	6.650
2B	3.075	5B	4.275	8B	5.475	BB	6.675
2C	3.100	5C	4.300	8C	5.500	BC	6.700
2D	3.125	5D	4.325	8D	5.525	BD	6.725
2E	3.150	5E	4.350	8E	5.550	BE	6.750
2F	3.175	5F	4.375	8F	5.575	BF	6.775

ELVDD Level – Address 0x02h [7:0] (Continued)

DAC Value	ELVDD(V)	DAC Value	ELVDD(V)	DAC Value	ELVDD(V)	DAC Value	ELVDD(V)
C0	6.800	D0	7.200	E0	7.600	F0	8.000
C1	6.825	D1	7.225	E1	7.625	F1	8.025
C2	6.850	D2	7.250	E2	7.650	F2	8.050
C3	6.875	D3	7.275	E3	7.675	F3	8.075
C4	6.900	D4	7.300	E4	7.700	F4	8.100
C5	6.925	D5	7.325	E5	7.725	F5	8.125
C6	6.950	D6	7.350	E6	7.750	F6	8.150
C7	6.975	D7	7.375	E7	7.775	F7	8.175
C8	7.000	D8	7.400	E8	7.800	F8	8.200
C9	7.025	D9	7.425	E9	7.825	F9	8.225
CA	7.050	DA	7.450	EA	7.850	FA	8.250
CB	7.075	DB	7.475	EB	7.875	FB	8.275
CC	7.100	DC	7.500	EC	7.900	FC	8.300
CD	7.125	DD	7.525	ED	7.925	FD	8.325
CE	7.150	DE	7.550	EE	7.950	FE	8.350
CF	7.175	DF	7.575	EF	7.975	FF	8.375

ELVSS Level – Address 0x03h [7:0]

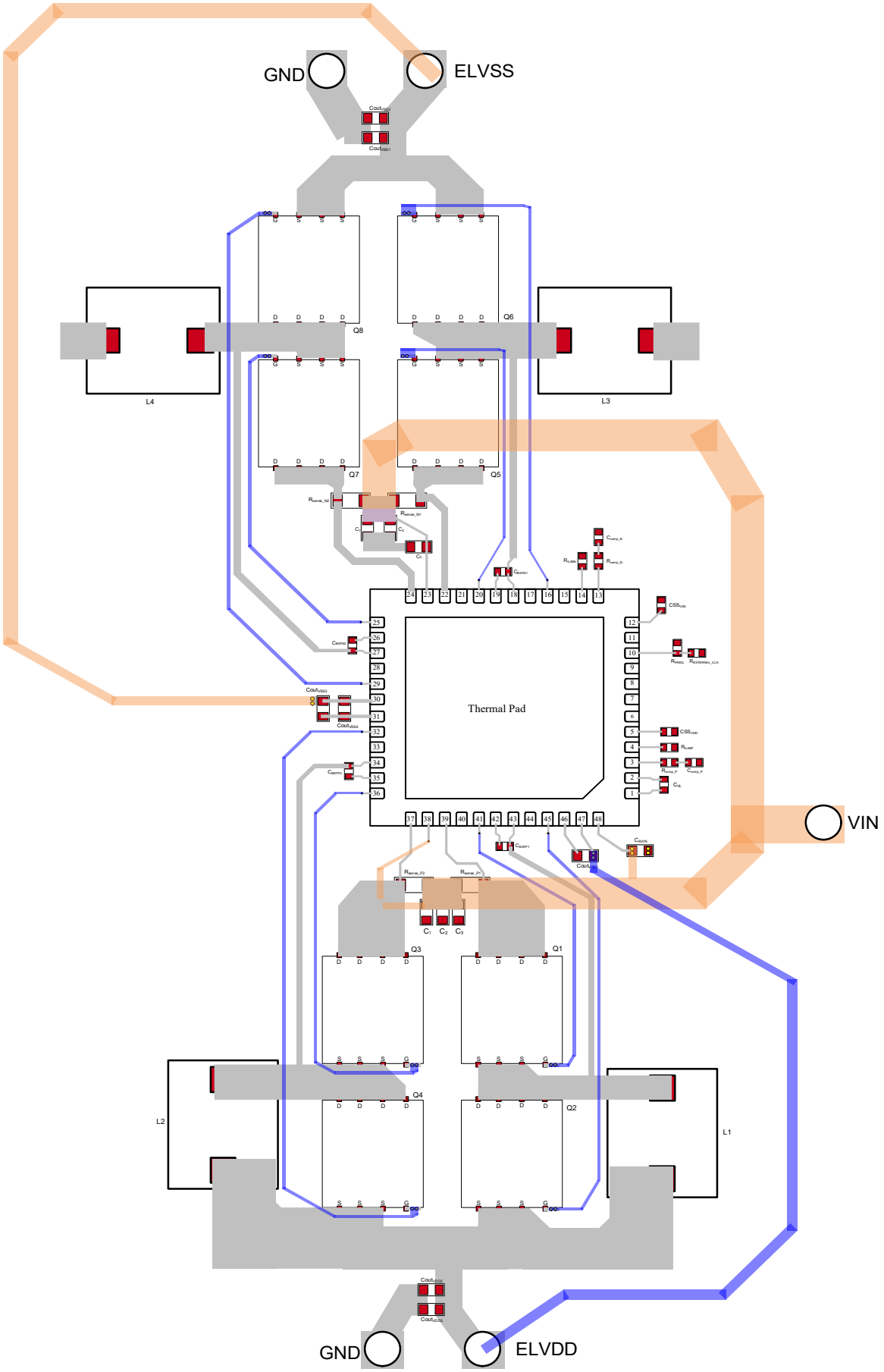
DAC Value	ELVSS(V)	DAC Value	ELVSS(V)	DAC Value	ELVSS(V)	DAC Value	ELVSS(V)
00	Disable	30	-8.70	60	-13.50	90	-18.00
01	-4.00	31	-8.80	61	-13.60	91	-18.00
02	-4.10	32	-8.90	62	-13.70	92	-18.00
03	-4.20	33	-9.00	63	-13.80	93	-18.00
04	-4.30	34	-9.10	64	-13.90	94	-18.00
05	-4.40	35	-9.20	65	-14.00	95	-18.00
06	-4.50	36	-9.30	66	-14.10	96	-18.00
07	-4.60	37	-9.40	67	-14.20	97	-18.00
08	-4.70	38	-9.50	68	-14.30	98	-18.00
09	-4.80	39	-9.60	69	-14.40	99	-18.00
0A	-4.90	3A	-9.70	6A	-14.50	9A	-18.00
0B	-5.00	3B	-9.80	6B	-14.60	9B	-18.00
0C	-5.10	3C	-9.90	6C	-14.70	9C	-18.00
0D	-5.20	3D	-10.00	6D	-14.80	9D	-18.00
0E	-5.30	3E	-10.10	6E	-14.90	9E	-18.00
0F	-5.40	3F	-10.20	6F	-15.00	9F	-18.00
10	-5.50	40	-10.30	70	-15.10	A0	-18.00
11	-5.60	41	-10.40	71	-15.20	A1	-18.00
12	-5.70	42	-10.50	72	-15.30	A2	-18.00
13	-5.80	43	-10.60	73	-15.40	A3	-18.00
14	-5.90	44	-10.70	74	-15.50	A4	-18.00
15	-6.00	45	-10.80	75	-15.60	A5	-18.00
16	-6.10	46	-10.90	76	-15.70	A6	-18.00
17	-6.20	47	-11.00	77	-15.80	A7	-18.00
18	-6.30	48	-11.10	78	-15.90	A8	-18.00
19	-6.40	49	-11.20	79	-16.00	A9	-18.00
1A	-6.50	4A	-11.30	7A	-16.10	AA	-18.00
1B	-6.60	4B	-11.40	7B	-16.20	AB	-18.00
1C	-6.70	4C	-11.50	7C	-16.30	AC	-18.00
1D	-6.80	4D	-11.60	7D	-16.40	AD	-18.00
1E	-6.90	4E	-11.70	7E	-16.50	AE	-18.00
1F	-7.00	4F	-11.80	7F	-16.60	AF	-18.00
20	-7.10	50	-11.90	80	-16.70	B0	-18.00
21	-7.20	51	-12.00	81	-16.80	B1	-18.00
22	-7.30	52	-12.10	82	-16.90	B2	-18.00
23	-7.40	53	-12.20	83	-17.00	B3	-18.00
24	-7.50	54	-12.30	84	-17.10	B4	-18.00
25	-7.60	55	-12.40	85	-17.20	B5	-18.00
26	-7.70	56	-12.50	86	-17.30	B6	-18.00
27	-7.80	57	-12.60	87	-17.40	B7	-18.00
28	-7.90	58	-12.70	88	-17.50	B8	-18.00
29	-8.00	59	-12.80	89	-17.60	B9	-18.00
2A	-8.10	5A	-12.90	8A	-17.70	B10	-18.00
2B	-8.20	5B	-13.00	8B	-17.80	B11	-18.00
2C	-8.30	5C	-13.10	8C	-17.90	…	-18.00
2D	-8.40	5D	-13.20	8D	-18.00	FD	-18.00
2E	-8.50	5E	-13.30	8E	-18.00	FE	-18.00
2F	-8.60	5F	-13.40	8F	-18.00	FF	-18.00

Layout Guideline

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the GQ2704A:

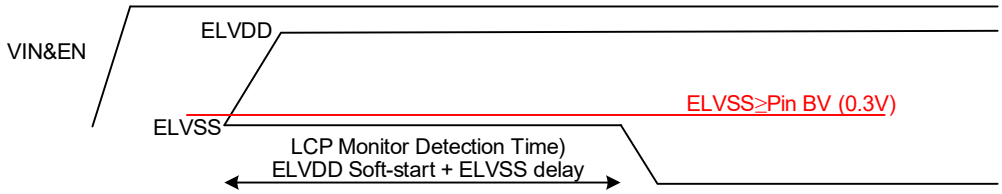
- Four-layer or six-layer PCB with maximum ground plane strongly recommended for good thermal performance.
- Keep the traces of the main current paths wide and short.
- Place the CAVIN as close to AVIN pin as possible.
- Place bootstrap capacitor, CBSTP1 / CBSTP2 / CBSTN1 / CBSTN2, as close to IC as possible.
- The high components away from SW and BOOT nodes should be as small as possible. Keep analog components away from the SW and BOOT nodes.
- Place the compensation components Rcomp_P / Ccomp_P/ Rcomp_N / Ccomp_N near the IC.
- Place the ELVSS output capacitors CoutELVSS3 / CoutELVSS4 near the IC.
- Q5 and Q7 current paths must be symmetrical.
- Q6 and Q8 current paths must be symmetrical.
- Q1 and Q3 current paths must be symmetrical.
- Q2 and Q4 current paths must be symmetrical.
- VIN high current path needs to go through C4 and C5 first.
- Place the C3 as close to VINN pin as possible.
- Place the CSS VDD 、CSS VSS as close to IC pin as possible.
- Place the R ILIMP 、R ILIMN as close to IC pin as possible.
- Place the ELVDD output capacitors CoutELVDD1 near the IC.
- VIN high current path needs to go through C1、C2 and C3 first.
- Place the R sense_P1、R sense_P2 and R sense_N1、R sense_N2 as close to IC pin as possible.
- It's recommended AGND to second layer.
- Keep PGND ground layer to top、third、bottom layer.

1. top layer to bottom layer



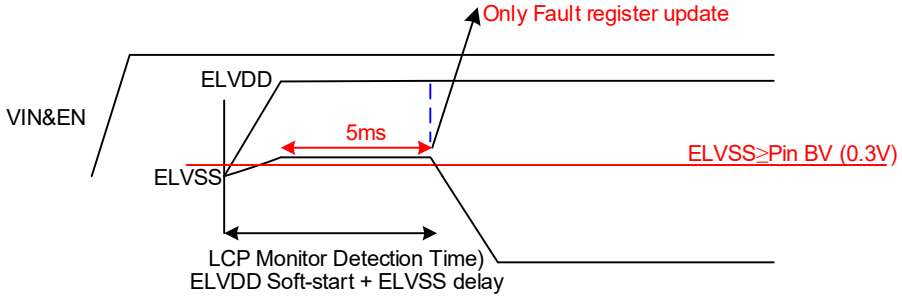
LCP Protection Indication:

(1) Normal power on case



Note: Detect time is accumulated

(2) Abnormal power on case

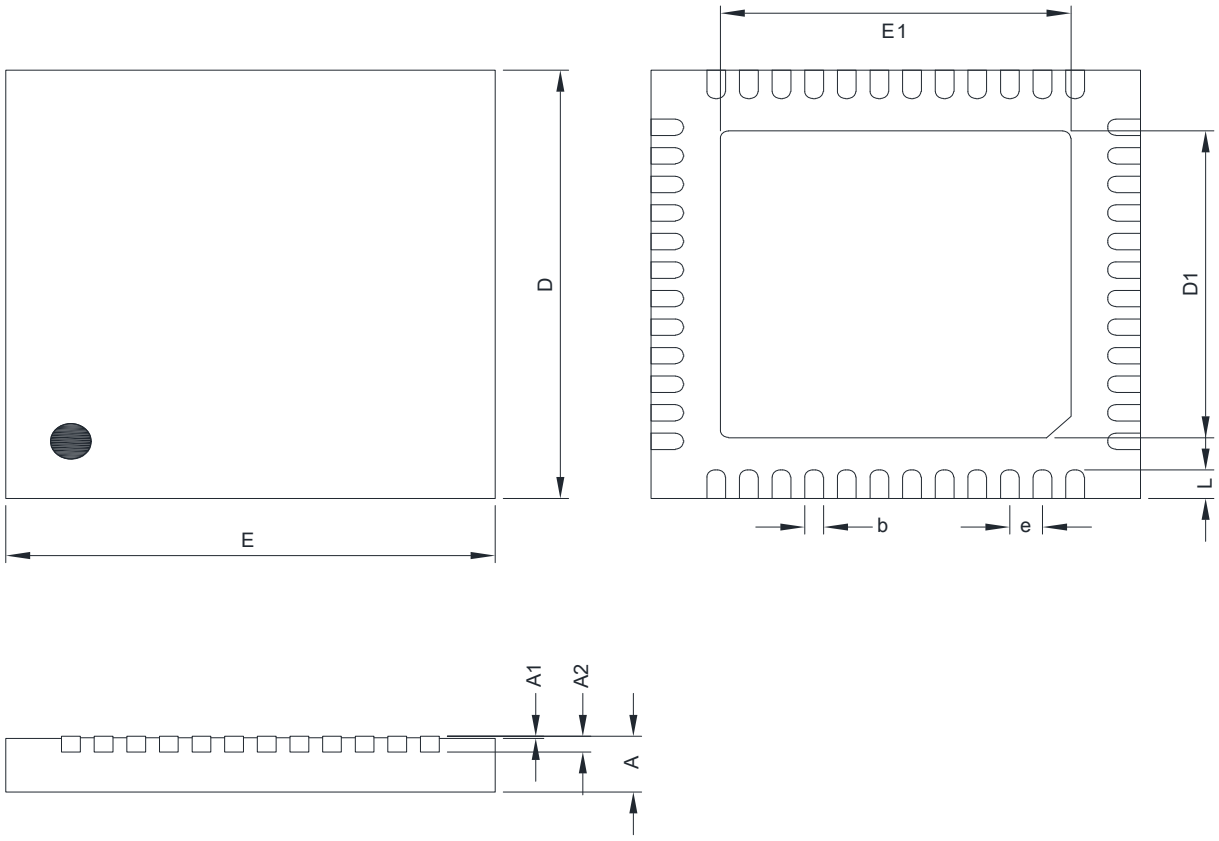


Note: Detect time is accumulated

Protections

Channel	Function	Working condition	ELVDD	ELVSS	PG	Released
General	UVLO	VIN < Falling UVLO (5.8V)	×	×	L	VIN Rising（0.3V Hysteresis）
	OTP	IC temp> 150°C	×	×	L	IC Temp under 130°C
	VIN OVP	VIN > 28V	×	×	L	VIIN<27V（1V Hysteresis）
ELVDD	UVP	V_{OUT} < Target value x 0.8 & delay 5ms	×	×	L	VIN or En Low
	SCP	V_{OUT} < Target value x 0.2 & delay 250μs	×	×	L	VIN or En Low
	OVP	V_{OUT} > Target value x 1.2	×	--	H	Normal Operating Voltage
	COMP	Comp >3.5V & delay 2s	×	×	L	VIN or En Low
ELVSS	UVP	V_{OUT} < Target value x 0.8 & delay 10ms	×	×	L	VIN or En Low
	SCP	V_{OUT} < Target value x 0.2 & delay 250μs	×	×	L	VIN or En Low
	OVP	V_{OUT} > Target value x 1.2	×	--	H	Normal Operating Voltage
	COMP	Comp >3.5V & delay 2s	×	×	L	VIN or En Low
	LCP	ELVSS pin≧0.3V & delay 5ms	H	H	H	Not latch off, only update fault register

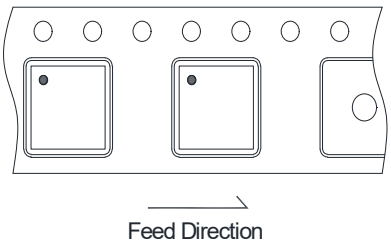
Package Information



TQFN6X6-48 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0.00	- - -	0.05	0.0000	- - -	0.0020
A2		0.20 REF			0.0079 REF	
D	5.95	6.00	6.05	0.2343	0.2362	0.2382
E	5.95	6.00	6.05	0.2343	0.2362	0.2382
D1	4.25	4.40	4.55	0.1673	0.1732	0.1791
E1	4.25	4.40	4.55	0.1673	0.1732	0.1791
b	0.13	0.20	0.25	0.0051	0.0079	0.0098
e		0.40 BSC			0.0157 BSC	
L	0.35	0.40	0.45	0.0138	0.0157	0.0177

Taping Specification



PACKAGE	Q'TY/REEL
TQFN6X6-48	3,000 ea